

Supporting Information for

# Fully Printed High-Performance n-Type Metal Oxide Thin-Film Transistors Utilizing Coffee-Ring Effect

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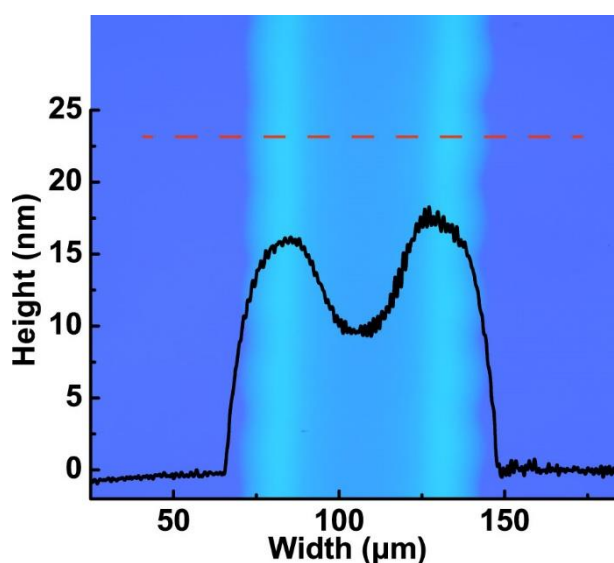
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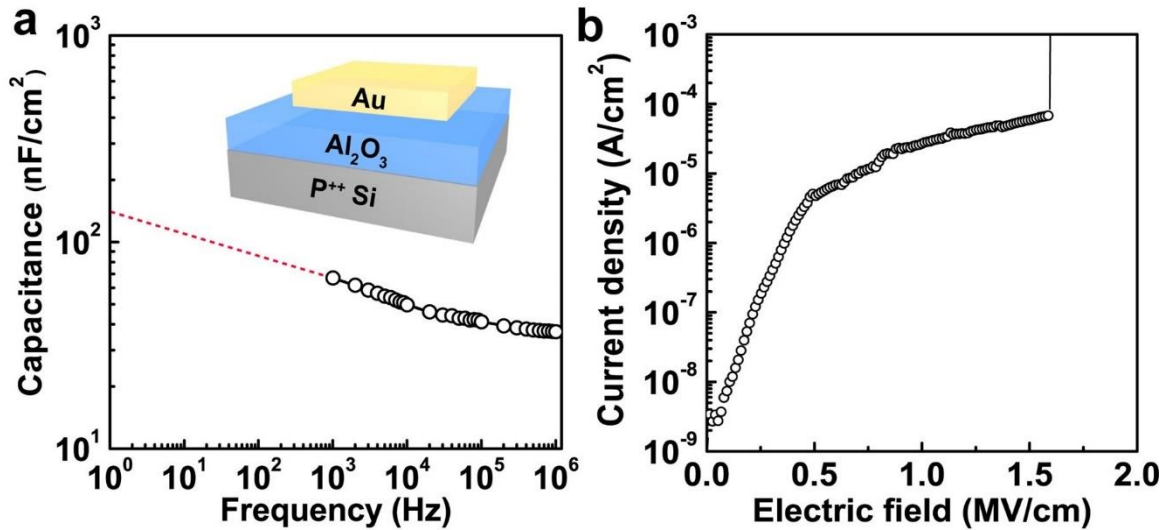
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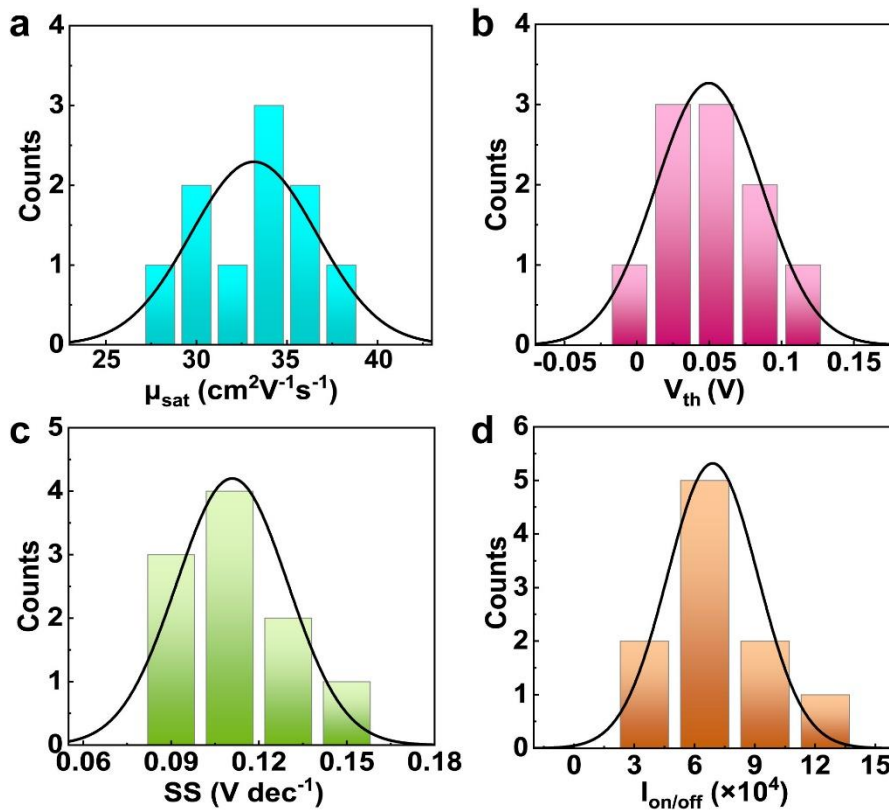
## Supplementary Tables and Figures



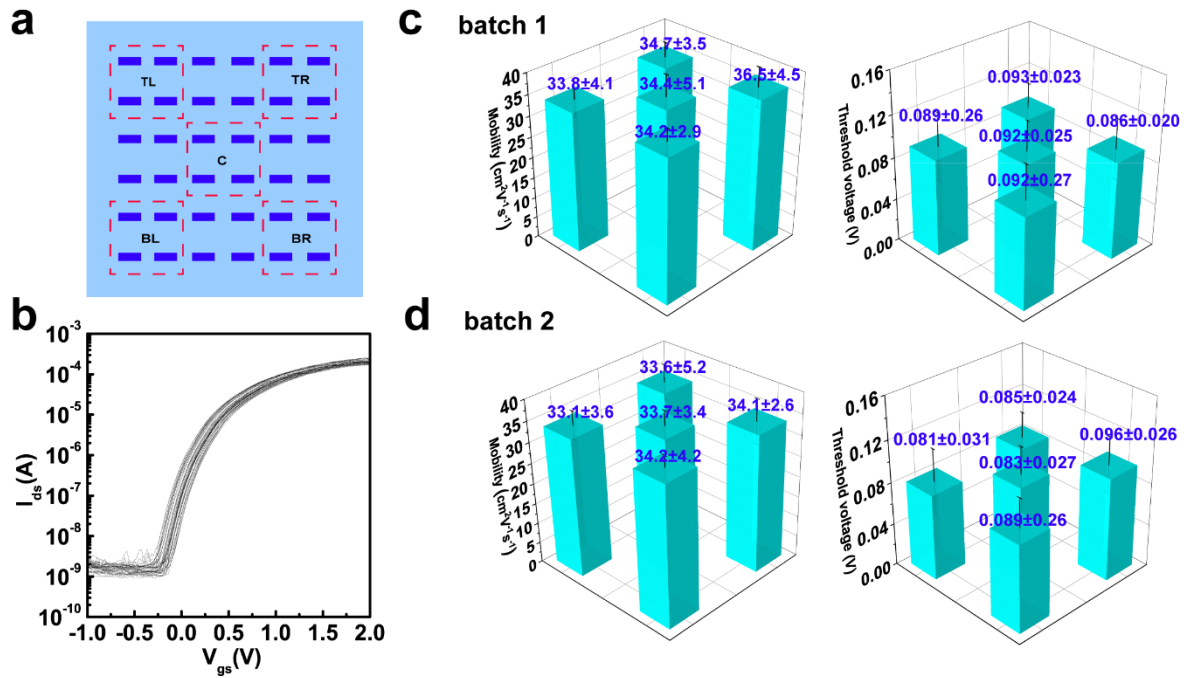
**Fig. S1** Optical image and height profile of printed ITO channel. The film was printed with 0.2 M ITO precursor ink, exhibiting typical coffee-ring effect where the center area is thinner than the edges.



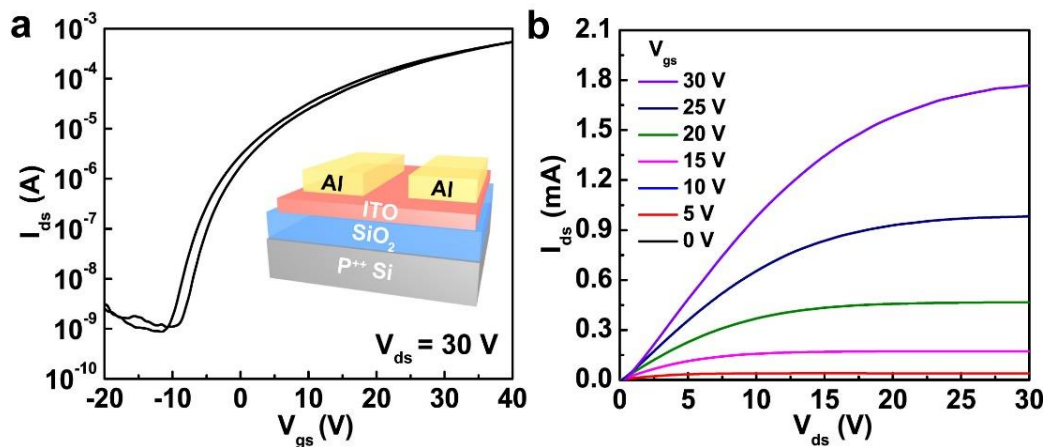
**Fig. S2** Electrical properties of printed Al<sub>2</sub>O<sub>3</sub> insulating layer based on a metal-insulator-metal (MIM) structure. (a) Areal capacitance of Al<sub>2</sub>O<sub>3</sub> film in the frequency range from 1 kHz to 1 MHz. The frequency-dependent capacitance behaviors may result from orientation polarization and space charge polarization in solution-processed Al<sub>2</sub>O<sub>3</sub> dielectric films. The capacitance of the printed Al<sub>2</sub>O<sub>3</sub> films was extrapolated to be 128 nF cm<sup>-2</sup> at 1 Hz. (b) Current density of the printed Al<sub>2</sub>O<sub>3</sub> dielectric with applied electric field. The tests were conducted based on a metal-insulator-metal structure with highly doped Si (*p*<sup>++</sup>) as bottom electrode, printed Al<sub>2</sub>O<sub>3</sub> as insulating layer, and thermal-evaporated Au films via shadow masks as patterned top electrodes. The device holds an area of 100 μm × 100 μm. The Al<sub>2</sub>O<sub>3</sub> film exhibited a low leakage current density of 2.3 × 10<sup>-5</sup> A cm<sup>-2</sup> at electric field strength of 1 MV/cm, and breakdown occurred until the electric field reached 1.6 MV cm<sup>-1</sup>.



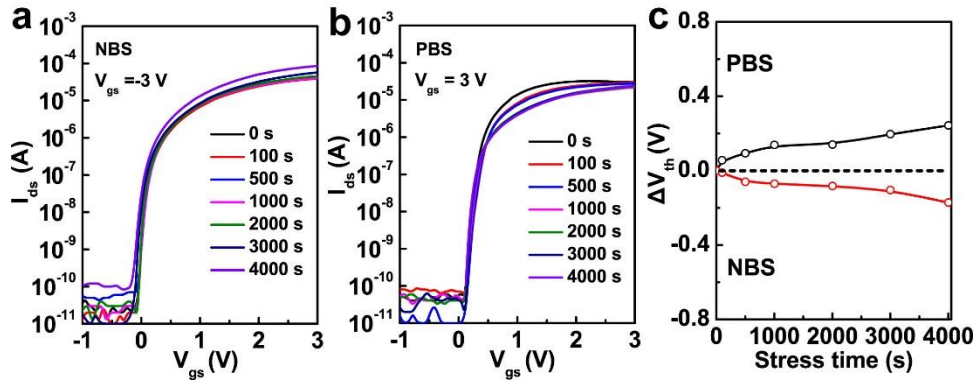
**Fig. S3.** Histograms showing the distribution of different parameters of the ITO TFTs. (a) Distribution of saturation mobility ( $\mu_{sat}$ ). (b) Distribution of threshold voltage ( $V_{th}$ ). (c) Distribution of subthreshold swing ( $SS$ ). (d) Distribution of current on/off ratios ( $I_{on/off}$ )



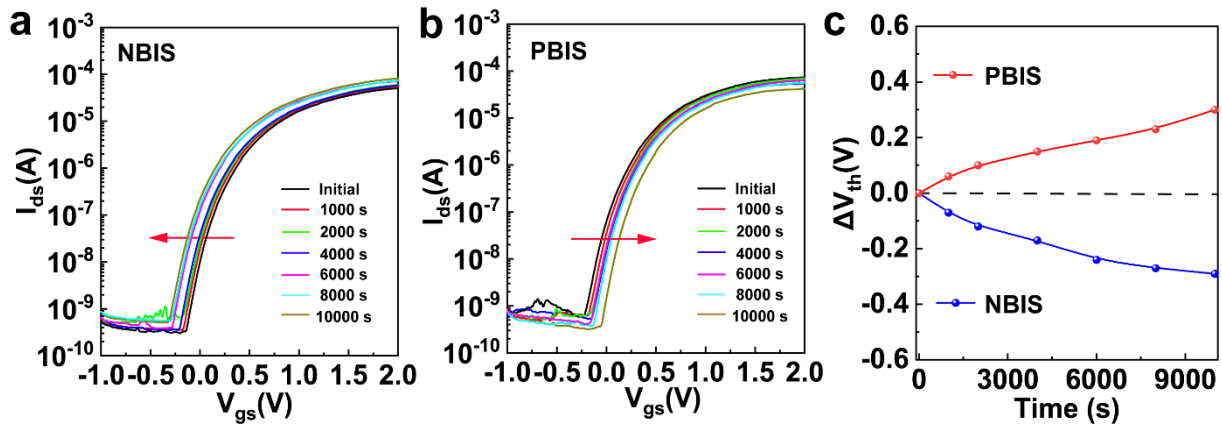
**Fig. S4** Probabilistic histograms of the mobility ( $\mu_{sat}$ ) and subthreshold voltage ( $V_{th}$ ) values of 40 printed devices from 2 batches. (a) Devices located at 5 different areas in each substrate were measured: top left (TL), top right (TR), bottom left (BL), bottom right (BR), and center area (C). 4 TFTs at each area were measured. In total, the parameters from 40 TFTs were collected (2 substrates  $\times$  5 area  $\times$  4 devices). (b) Transfer curves for all statistical devices. (c-d) Average  $\mu_{sat}$  and  $V_{th}$  values from two batches, showing high uniformity with deviations less than 15%



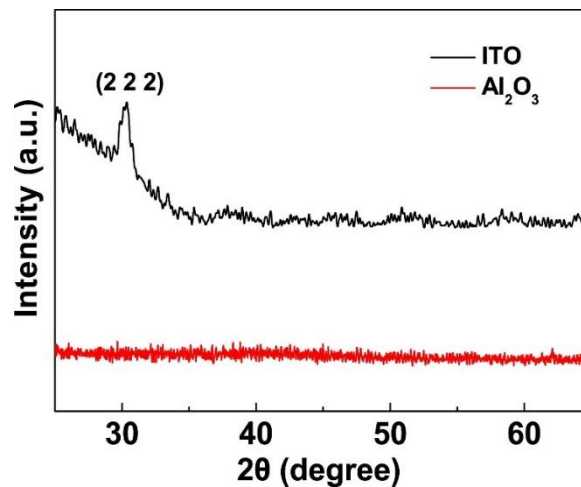
**Fig. S5** The electrical characteristics of ITO TFTs on Si/SiO<sub>2</sub> substrates. Transfer (a) and output characteristics (b) of printed ITO TFTs fabricated on Si substrate with 100 nm thick SiO<sub>2</sub> gate dielectric with annealing temperature of 350 °C in air. The device exhibited electrical properties with  $\mu_{sat} = 11.8 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ ,  $V_{th} = 2.2 \text{ V}$ ,  $SS = 1.5 \text{ V dec}^{-1}$ ,  $I_{on/off} = 5.2 \times 10^5$ , and  $D_{it} = 5.3 \times 10^{12} \text{ cm}^{-2} \text{eV}^{-1}$ . S/D electrodes of 50 nm thick Al was thermally evaporated via a shadow mask, forming channel L/W = 200/1000  $\mu\text{m}$ .



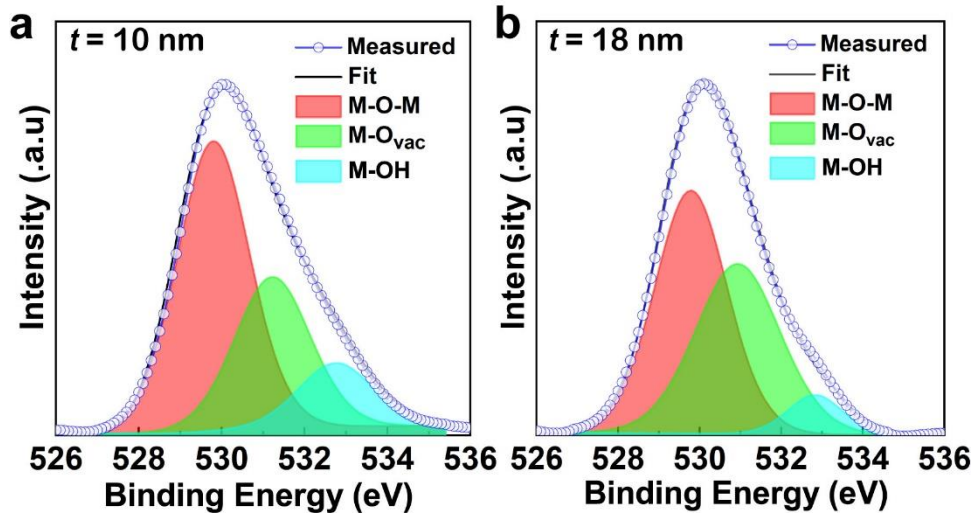
**Fig. S6** Electrical stability of fully printed ITO TFTs. (a, b) Time-dependent transfer curves of the fully printed ITO TFTs under NBS ( $V_{gs} = -3$  V) (a) and PBS ( $V_{gs} = 3$  V) (b). (c) The detailed plots of threshold voltage shifts ( $\Delta V_{th}$ ) as a function of stress time of the ITO TFT. The negative shift of  $V_{th}$  under NBS can be attributed to the attraction of oxygen vacancies at the channel/dielectric interface and the repelling of electrons towards back channel. And the positive shift under PBS results from the electron trapping at or near the active channel/dielectric interfaces.



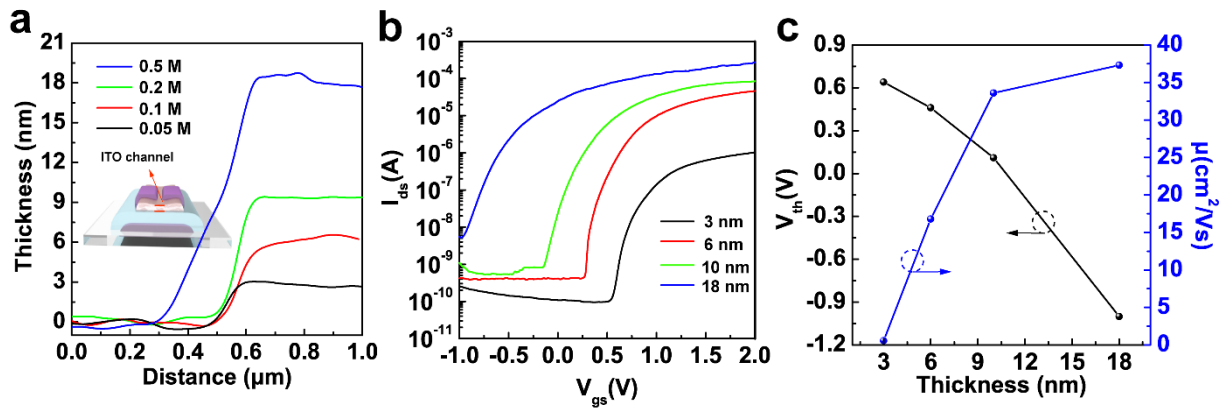
**Fig. S7** Electrical stability of fully printed ITO TFTs under white light illumination. Evolution of transfer curves of the ITO TFTs as a function of (a) NBIS and (b) PBIS. (c) Threshold voltage shifts ( $\Delta V_{th}$ ) as a function of bias stress time. The NBIS/PBIS was performed in air at room temperature under white LED light illumination (3000 lux), and the applied gate bias was  $-/+$  1 V, respectively.



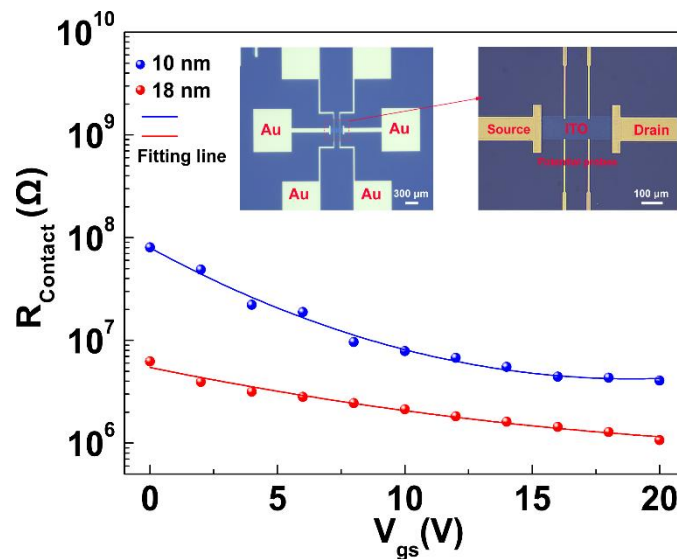
**Fig. S8** X-ray diffraction patterns of printed ITO and  $Al_2O_3$  films on  $SiO_2$  substrates. The XRD patterns revealed the printed ITO film is polycrystalline and  $Al_2O_3$  film is amorphous.



**Fig. S9** XPS analysis of ITO films with different thicknesses. XPS O-1s spectra collected from printed (a) ITO channel (10 nm thick) and (b) ITO contacts (18 nm thick) films

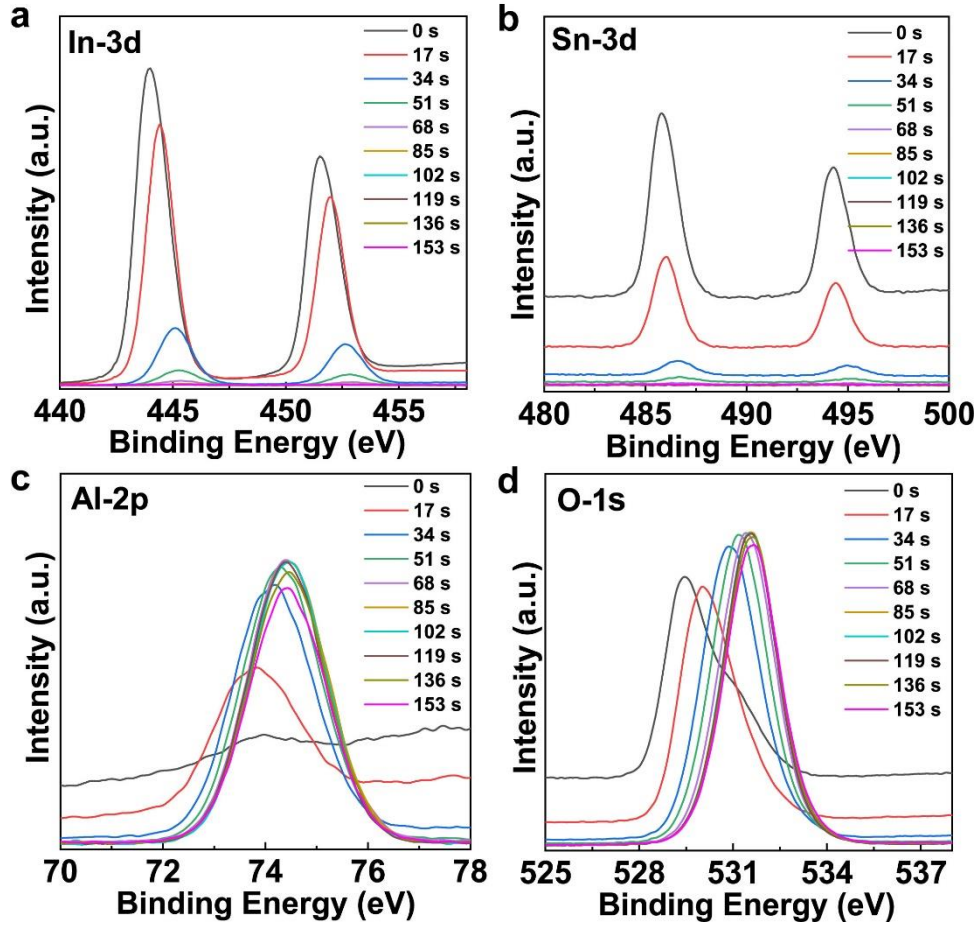


**Fig. S10** The electrical characteristics of ITO TFTs with different channel thicknesses. (a) Cross-sectional scanning of ITO channel films by AFM. Inset illustrates the structure of the fully printed TFT. (b) Transfer curves of fully-printed TFTs with different channel thicknesses. (c) Extracted  $\mu_{sat}$  and  $V_{th}$  as a function of ITO thickness



**Fig. S11** Analysis of contact resistivity by gated four-probe (GFP) measurements. ITO channel was spin-coated on Si/SiO<sub>2</sub> substrate and patterned by photolithography and wet etching. Cr/Au (3/30 nm) electrodes were patterned and deposited via e-beam evaporation.

The contact resistance between the 10 nm, 18 nm ITO channel and the Cr/Au electrode decreases with the increase of the gate voltage. Thicker ITO has lower contact resistance. Inset illustrates optical images of the ITO GFP devices.



**Fig. S12** XPS depth profile of the ITO/ $\text{Al}_2\text{O}_3$  heterostructures as a function of etching time. (a) In-3d, (b) Sn-3d (c) Al-2p, and (d) O-1s core-level XPS spectra of the ITO/ $\text{Al}_2\text{O}_3$  films, where the intensities of In-3d and Sn-3d peaks decrease with time while that of Al-2p shows opposite trend.

**Table S1** Comparison of inverters performance based on solution-processed metal oxide TFTs

Deposition method	Channel materials	Inverter load	$V_{\text{dd}}$ (V)	Gain (V/V)	References
	$\text{In}_2\text{O}_3$	Resistor	4	9.7	[S1]
	$\text{In}_2\text{O}_3$	Resistor	2.5	5	[S2]
	$\text{In}_2\text{O}_3$	Resistor	3	6	[S3]
Spin-coating	$\text{In}_2\text{O}_3$	Resistor	10	10.6	[S4]
	ZTO	CMOS	40	10	[S5]
	ZTO	NMOS	15	23.2	[S6]
	ZTO	Resistor	2.5	7.3	[S7]

	ZnO	CMOS	1	18	[S8]
	IZO	Resistor	4	4.46	[S9]
	IGZO	CMOS	40	50	[S10]
	IGZO	CMOS	50	5	[S11]
	IGZO	NMOS	10	1.83	[S12]
	ZnO	NMOS	15	70	[S13]
	IGZO	Resistor	5	19.8	[S14]
	In <sub>2</sub> O <sub>3</sub>	CMOS	1.5	18	[S15]
	In <sub>2</sub> O <sub>3</sub>	Resistor	4	16	[S16]
	In <sub>2</sub> O <sub>3</sub>	CMOS	1.5	21	[S17]
Inkjet-printing	ZnO	Resistor	2	8	[S18]
	IGZO	CMOS	10.5	12	[S19]
	In <sub>2</sub> O <sub>3</sub>	NMOS	20	45	[S20]
	IGZO	NMOS	0.5	2.5	[S21]
Fully-printing	IGO	Resistor	2	5	[S22]
	ITO	NMOS	3	181	<b>This work</b>

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