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Efficient CNTFET-based Ternary Full Adder Cells for Nanoelectronics

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Abstract: This paper presents two new efficient ternary Full Adder cells for nanoelectronics. These CNTFET-based ternary Full Adders are designed based on the unique characteristics of the CNTFET device, such as the capability of setting the desired threshold voltages by adopting proper diameters for the nanotubes as well as the same carrier mobilities for the N-type and P-type devices. These characteristics of CNTFETs make them very suitable for designing high-performance multiple-V_{th} structures. The proposed structures reduce the number of the transistors considerably and have very high driving capability. The presented ternary Full Adders are simulated using Synopsys HSPICE with 32 nm CNTFET technology to evaluate their performance and to confirm their correct operation.
Keywords: CNTFET; Multiple-Valued logic; Ternary logic; Ternary Full Adder; Multiple-V_{th} design

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Introduction

Complementary Metal Oxide Semiconductor (CMOS) process has been the dominant technology, which provides the needed size scaling for implementing low-power, high-performance and high-density VLSI circuits and systems. At the present time, nearly all the human activities are dependent upon CMOS technology and majority of the indispensible daily applications, such as financing, telecommunication, transportation, education and medical care would stop working without this technology. Nevertheless, this technology encounters many critical challenges and difficulties due to the unavoidable scaling down of the dimension of the MOS transistors deeper in nanoscale. These problems, such as high power density, reduced gate control, parameter deviations and very high lithography costs, hinder this continuous scaling and consequently reduce the suitability of the CMOS technology for the high-performance applications, in the upcoming future. To alleviate these difficulties, some beyond-CMOS nanodevices such as Carbon Nanotube Field Effect Transistor (CNTFET), Single Electron Transistor (SET), Graphene Nanoribbon Transistor (GNRT) and Quantum-dot Cellular Automata (QCA) have been proposed as the possible alternatives to replace the conventional bulk CMOS in the near future [1]. However, considering all of these nanodevices, CNTFET could be more of an interest due to its similarities with MOSFET in terms of inherent electronic properties. Due to these similarities, previously designed CMOS architectures and basic CMOS-based platforms can still

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be used without any major modifications. In addition, the unique one-dimensional band-structure of the CNTFET device suppresses backscattering and causes near-ballistic operation, which leads to very high-speed operation [2]. The CNTFET nanodevice is generally faster and has less power consumption compare to the bulk silicon transistors and is more suitable for high-frequency and low-voltage applications.

In recent years, many CNTFET-based circuits such as CNTFET-based binary Full Adders [3], and Multiple-valued logic and arithmetic circuits [4-6] have been proposed in the literature. Nevertheless, among these structures, Multiple-valued Logic (MVL) design could be more of an interest in the CNTFET nanotechnology. This is because the most suitable method for designing voltage-mode MVL circuits is the multiple-threshold (multi-V_{th}) design technique and the required threshold voltage can be obtained just by adopting proper diameters for the nanotubes of the CNTFET device [4-6].

Unlike binary logic, in MVL systems more than two logic levels are permitted and arithmetic and logical operations could be carried out on more than two authorized logic values. Therefore, by using MVL, many logical and arithmetic operations could be executed with higher speed and smaller number of computation stages [6]. The main challenges of the binary logic in designing large and dense chips are pin-out and interconnection problems that limit the number of connections outside and inside of the circuits [7]. Moreover, many real life applications, such as process control and robotics can be implemented more efficiently by using MVL systems. Using MVL leads to chips with less complexity and smaller area as well as very high-bandwidth parallel and serial data transfer. Among the radices greater than two, the radix-e ($e \simeq 2.718$) logic results in the most efficient implementation of the MVL systems [8]. However, due to the restrictions in implementation of the real systems, hardware designers are limited to only use the natural numbers as the base of computation. The most efficient multiple-valued system, which leads to the least product cost and complexity, is the ternary logic [6].

On the other hand, one of the most consequential parts of many VLSI applications, such as microprocessors, video and image processing and DSP architectures is the arithmetic unit [9]. The most fundamental arithmetic circuit which is the building block of the arithmetic unit is commonly the Full Adder cell. Therefore, to design and implement high-performance ternary VLSI systems, efficient ternary Full Adder cells are in high demand. Unfortunately, due to the hardware inefficiency of designing ternary Full Adder cell based on the conventional CMOS design methods, some effort has already been made for designing this important circuit.

In this paper two efficient ternary Full Adder cells are proposed exclusively for CNFET nanotechnology, which are based on a different design style with respect to the other ternary circuits, previously presented in the literature. The proposed circuits are designed based on the unique properties of CNFETs, such as the capability of CNTs, to be configured to have the desired threshold voltages depending on their diameter, which is not feasible in CMOS technology. These novel designs have less complex structures and much less number of transistors, compared to the conventional ternary arithmetic circuits.

In Section 2 of this paper, a brief review of CNTFET devices is presented. The new CNTFET-based ternary Full Adders are presented in Section 3. Section 4 includes the experimental result and finally, Section 5 concludes the paper.

Review of Carbon Nanotube Field Effect Transistors (CNTFETs)

Carbon Nanotube (CNT), discovered in 1991 by S. Iijima [10], is a nano-scale tube created as a rolled sheet of graphite. CNTs can be multi-walled (MWCNT) or single-walled (SWCNT) [11]. A MWCNT is composed of more than one cylinder whereas a SWCNT is comprised of a single cylinder. A SWCNT could be semiconductor or conductor, being contingent upon its chirality vector. The chirality vector, which is the wrapping vector that the graphite sheet is rolled up along it, is determined by (n_1, n_2) indices. These indices specify the arrangement angle of the carbon atoms along the nanotube. If $n_1 - n_2 \neq 3k$ ($k \in \mathbb{Z}$), the SWCNT is semiconductor and otherwise it is metallic [2]. If $n_1 = n_2$, the SWCNT is called to have the Armchair structure, and hence a SWCNT with the Armchair structure is always metallic. If $n_1 = 0$ or $n_2 = 0$, the SWCNT is called to have the Zigzag structure, hence the Zigzag SWCNTs with $n_1 \neq 3k$ or $n_2 \neq 3k$ ($k \in \mathbb{Z}$) are semiconductor. For the other (n_1, n_2) pairs, SWCNTs have the Chiral structure. In a CNTFET device one or more semiconducting SWCNTs are used as the channel of the device. Besides the unique properties of the CNT material, removing the channel from the silicon bulk leads to elimination and reduction of many parasitic elements.

Moreover, the current-voltage ($I-V$) characteristics of the MOSFET and CNTFET devices are alike. CNTFET also has P-type and N-type devices like MOSFET. However, unlike the MOSFET devices, P-CNTFET and N-CNTFET devices with same geometries have same mobilities ($m_n = m_p$) and as a result same drive capabilities. These unique characteristics are very consequential for simplifying the design and transistor sizing procedures of complex CNTFET-based circuits [12]. Another great merit of carbon nanotube technology is

the possibility of using high-density and linear Carbon Nanotube Capacitors (CNCAPs) [13]. This capacitor is much denser and demonstrates a lot better electrical characteristics compared to the conventional CMOS on-chip capacitors, such as MOSCAPs or MIMCAPs.

In general, CNTFET has higher ON current compared to MOSFET for the same OFF current. Due to the small molecular structure of the CNTFET device, scaling the future size, beyond what currently available advanced lithographic methods permit, is possible. In addition due to the fact that CNT does not have surface dangling bonds as Silicon, some other amorphous or crystalline insulators can be used instead of SiO_2 in the structure of CNTFETs. Ballistic conduction of the CNT decreases the power dissipation in the body of CNTFET, increases the speed of the device considerably and makes it suitable for low-voltage, low-power and very high speed and applications. Moreover, one dimensional structure of CNTs lowers the resistivity which leads to energy consumption minimization and consequently reduction of the power consumption density in the channel of CNTFET. Besides the stated advantages of the CNTFETs in comparison with the classical bulk MOSFETs, it also encounters some challenges, such as the problems in the fabrication process of CNTFETs on the currently available CMOS platforms. For example, in the integration procedure, local-gate CNTFET is demanded. However, most of the local-gate designs use metal as the gate and it is quite difficult to combine the metal gate and the grown CNTs for the integration due to the metal melting point limit [14]. In addition, since carbon nanotube network films are comprised of both metallic and semiconducting CNTs, some CNTFETs fabricated on the basis of CNT network films may not turn off completely, which can be troublesome for VLSI applications. However, encouraging research endeavor is being performed to solve these physical problems and challenges in the upcoming future [15].

In the structure of a CNTFET device (see Fig. 1(a)), the distance between the centers of two adjoining nanotube channels under the same gate of a CNTFET is called a pitch, which considerably affects the width of the gate and the contacts of the transistor. The width of the gate of a CNTFET can be estimated based on the following equation [16]:

$$W_{\text{gate}} \simeq Min(W_{\text{min}}, N\,\text{Pitch}) \qquad (1)$$

where, N is the number of nanotubes under the gate and W_{min} is the minimum width of the gate. Similar to MOSFET, a CNTFET device has also threshold voltage (V_{th}) which is the voltage needed for turning on the transistor electrostatically via the gate. Another great advantage of CNTFET device is that its threshold voltage can be determined just by adopting a proper diameter for its CNTs. This practical attribute makes CNTFET more flexible than MOSFET for designing digital circuits and makes it very suitable for designing multi-V_{th} circuits. The threshold voltage of a CNTFET is approximately considered as the half bandgap and can be calculated by the following equation [16]:

$$V_{\text{th}} \simeq \frac{E_{\text{g}}}{2e} = \frac{\sqrt{3}}{3}\frac{aV_{\pi}}{eD_{\text{CNT}}} \simeq \frac{0.43}{D_{\text{CNT}}(\text{nm})} \qquad (2)$$

where, V_{π} ($\simeq$3.033 eV) is the carbon $\pi-\pi$ bond energy in the tight bonding model, a ($\simeq$ 0.249 nm) is the carbon to carbon atom distance, D_{CNT} is the diameter of CNT and e is the unit electron charge. It can be concluded from Equation (2) that the threshold voltage of a CNTFET is an inverse function of the diameter of its CNTs, which can be calculated by the following equation [16]:

$$D_{\text{CNT}} = \frac{a\sqrt{n_1^2+n_2^2+n_1n_2}}{\pi} \simeq 0.0783\sqrt{n_1^2+n_2^2+n_1n_2} \qquad (3)$$

For example, for a CNTFET with the chiral numbers (n_1, n_2) = (10, 0), D_{CNT} is 0.783 nm and subsequently its threshold voltages is 0.557 V.

Three distinctive types of CNTFETs have already been introduced in the literature. The first one is Schottky Barrier CNTFET (SB-CNTFET), which is shown in Fig. 1(b). SB-CNTFET is a tunneling transistor and performs on the principles of direct tunneling via a Schottky Barrier (SB) at the source/drain-channel junction. The energy barrier at SB actually limits the transconductance of the CNTFET in the ON state and decreases the drain current (I_{d}), which is a consequential parameter for high-speed operation. Moreover, SB-CNTFETs have strong ambipolar attributes that limits the usage of these devices in conventional CMOS architectures. To eliminate the stated drawback of SB-CNTFET, some efforts have been made to fabricate CNTFETs, which works similar to normal MOSFETs but with higher speed and lower energy consumption. Therefore, Potassium doped drain and source CNT regions have been fabricated and the field-effect behaviour and unipolar attributes have been achieved. The main profit of this kind of device which is called MOSFET-like CNTFET (see Fig. 1(c)) is that its source/drain-channel junction has no Schottky Barrier. As a result, it has considerably higher ON current and consequently MOSFET-like CNTFETs are very suitable for ultra high-performance applications. The third type of CNTFET, called the band-to-band tunneling CNTFET (T-CNTFET), which is demonstrated in Fig. 1(d), has super cut-off characteristics and low ON currents. T-CNTFET is very appropriate for ultra-low-power and subthreshold circuit designing [17-19].

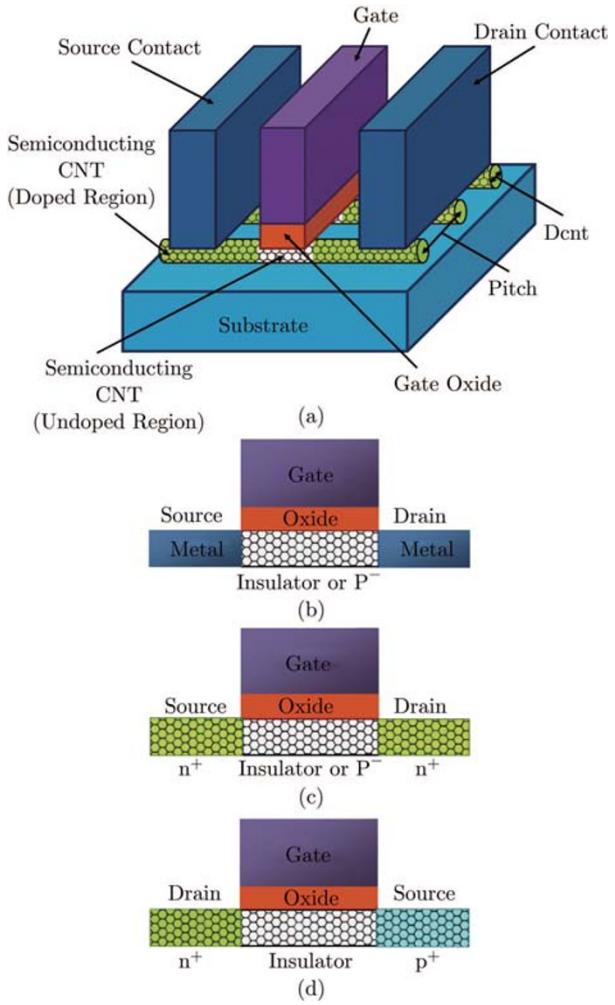

Fig. 1 (a) A typical CNTFET device; Different types of CNTFET device (b) SB-CNTFET (c) MOSFET-like CNTFET (d) T-CNTFET.

Based on the stated advantages and disadvantages of the various types of CNTFETs and also due to the more similarities between MOSFET-like CNTFETs and MOSFETs in terms of inherent characteristics and operation, this type of CNTFET is utilized for designing the proposed ternary Full Adder cells.

The Proposed Ternary Full Adder Cells

Ternary logic is a type of MVL, which consists of three significant logic values. These logic values can be symbolized into "0", "1" and "2", which are equivalent to 0, $1/2V_{DD}$, and V_{DD} voltage values. The most fundamental ternary arithmetic circuit is the 1-trit ternary Full Adder cell. The truth table of a 1-trit ternary Full Adder cell with A, B, C_{in} (input carry) inputs and Sum and C_{out} (output carry) outputs is shown in Table 1.

According to Table 1, the relation between the input and output of a ternary Full Adder cell can be presented by the following equation:

$$A + B + C_{\text{in}} = \sum \text{in} = 3C_{\text{out}} + \text{Sum} \tag{4}$$

By dividing both sides of Eq. 4 by 3, it can be considered as follows:

$$\frac{\sum \text{in}}{3} = C_{\text{out}} + \frac{\text{Sum}}{3} \tag{5}$$

Table 1 Truth table of a 1-trit ternary Full Adder cell.

$\sum \text{in} = A + B + C_{\text{in}}$	C_{out}	$\overline{C_{\text{out}}}$	Sum	$\overline{\text{Sum}}$
0	0	2	0	2
1	0	2	1	1
2	0	2	2	0
3	1	1	0	2
4	1	1	1	1
5	1	1	2	0
6	2	0	0	2

As a result,

$$\left\lfloor \frac{\sum \text{in}}{3} \right\rfloor = \left\lfloor C_{\text{out}} + \frac{\text{Sum}}{3} \right\rfloor \tag{6}$$

where, $\lfloor\rfloor$ symbol denotes the floor function and results the integer part of the expression inside it. Since $0 \leq \text{Sum}/3 < 1$ and $C_{\text{out}} \in \{\mathbb{N}, 0\}$, Eq. 6 could be considered as the following equation, which results the C_{out} output:

$$C_{\text{out}} = \left\lfloor \frac{\sum \text{in}}{3} \right\rfloor \tag{7}$$

$\overline{C}_{\text{out}}$ which is the 2's complement of C_{out} is defined by the following equation:

$$\overline{C_{\text{out}}} = 2 - C_{\text{out}} \tag{8}$$

Therefore,

$$C_{\text{out}} = 2 - \overline{C_{\text{out}}} \tag{9}$$

By considering both Eq. 4 and Eq. 9 the following relations are obtained, which result the Sum output:

$$\sum \text{in} = 3\,(2 - C_{\text{out}}) + \text{Sum} \tag{10}$$

$$\text{Sum} = \sum \text{in} + 3\overline{C_{\text{out}}} - 6 \tag{11}$$

The proposed ternary Full Adder cells are indeed the efficient hardware implementations of both Eq. 7 and Eq. 11. The C_{out} signal can be implemented according to Eq. 7 by utilizing the capacitor-based scaled analog summation for producing $\frac{\sum \text{in}}{3}$ together with a ternary buffer [4] with proper threshold values for implementing the floor function. The proposed structure for generating the ternary C_{out} signal is demonstrated in Fig. 2. It is worth mentioning that the ternary buffer is indeed two cascaded ternary inverters, in which the first inverter is the threshold detector block for implementing the floor function and the second one is a standard

ternary inverter that produces the C_{out} signal from the generated $\overline{C_{\text{out}}}$. It is also notable that the thresholds of the ternary threshold detector circuit can be adjusted by choosing proper threshold voltages for its binary CNTFET-based inverters which is exactly equivalent to adopting proper diameters for the channels of the CNTFETs according to Eq. 2.

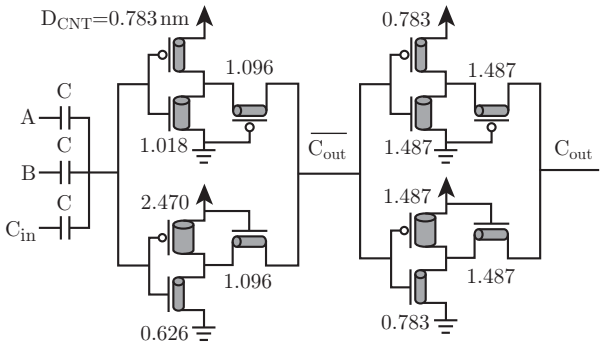

Fig. 2 The ternary C_{out} generator module.

For designing the ternary Sum generator, Eq. 11 can be rewritten as follows:

$$\text{Sum} = 6\left(\underbrace{\frac{\frac{\sum \text{in}}{3} + \overline{C_{\text{out}}}}{2}}_{S} - 1\right) \tag{12}$$

The S term in Eq. 12 can be implemented by using a proper capacitor-based scaled analog summation. Moreover, the $6(S-1)$ relation can be implemented indirectly by utilizing a ternary inverter as a threshold detector together with a standard ternary inverter. The proposed ternary Sum signal generator is shown in Fig. 3.

The complete ternary Full Adder cell, which is a combination of the circuits of Fig. 2 and Fig. 3 and is composed of only 24 CNTFETs and 5 capacitors (C_1=3 fF and C_2=0.7 fF), is shown in Fig. 4. The structure of the proposed ternary Full Adder cell is simple and modular. Moreover, this cell generates all the Sum, C_{out}, $\overline{\text{Sum}}$ and $\overline{C_{\text{out}}}$ signals.

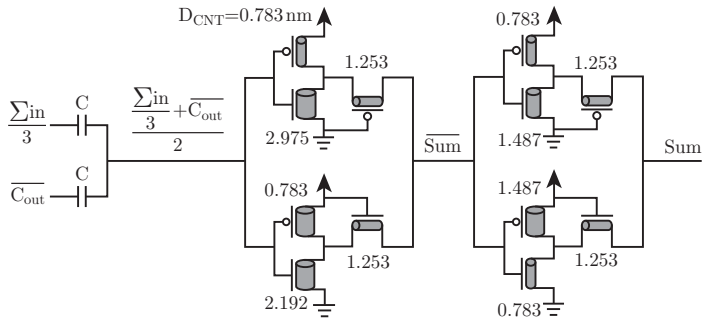

Fig. 3 The ternary Sum generator module.

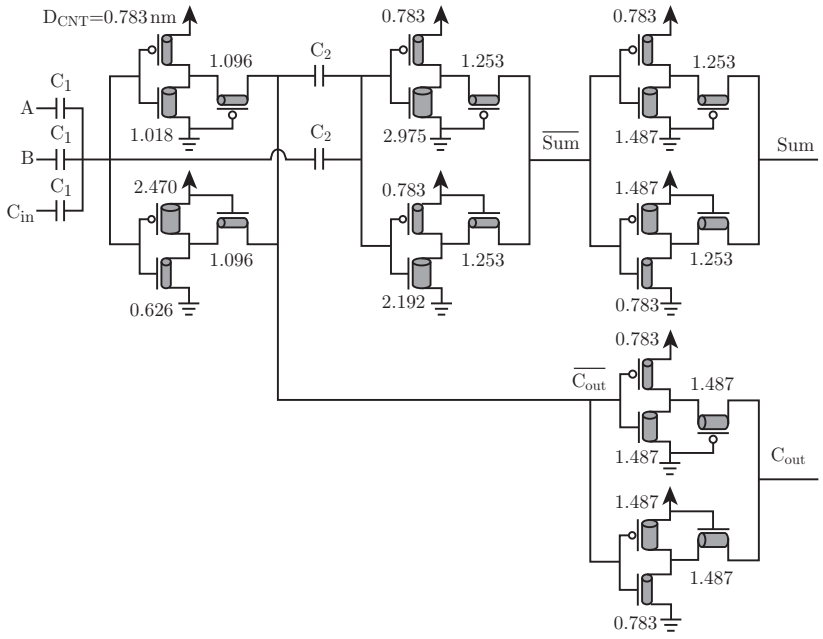

Fig. 4 The first proposed ternary Full Adder cell.

The number of the CNTFETs of the proposed ternary Full Adder cell could be reduced by utilizing a direct ternary buffer [4], instead of two cascaded ternary inverters, as the threshold detector for generating the Sum signal. This new structure, which is composed of only 18 CNTFETs and 5 capacitors, is shown in Fig. 5.

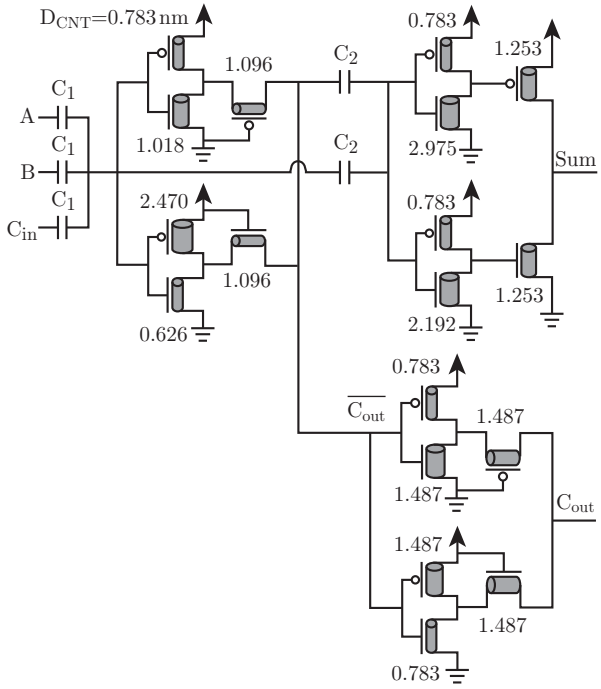

Fig. 5 The second proposed ternary Full Adder cell.

It is worth mentioning that the proposed method of designing ternary structures significantly reduces the number of the transistors of the ternary Full Adder cell and do not require any additional power supplies. For instance the conventional CMOS ternary Full Adder cell [20] is composed of more than 200 transistors and needs an additional voltage supply. As an another instance the state-of-the-art CNTFET-based ternary Full Adder cell, which can be considered as two cascaded CNTFET-based ternary Half Adders [6] is composed of 190 CNTFETs and requires an extra voltage supply.

Simulation Results

In this section, the proposed ternary Full Adder cells are examined extensively in various conditions, using Synopsys HSPICE simulator with the Compact SPICE Model for CNTFETs (Lg=32 nm), including the possible nonidealities [21,22]. This standard model has been designed for unipolar enhancement-mode MOSFET-like CNFET devices, in which each transistor may include one or more CNTs as its channel. This model also considers a realistic, circuit-compatible CNFET structure and includes practical device nonidealities, parasitics, Schottky-barrier effects at the contacts, inter-CNT charge screening effects, doped source-drain extension regions, scattering (nonideal near-ballistic transport), back-gate (substrate bias) effect and Source/Drain, and Gate resistances and capacitances. The model also includes a full transcapacitance network for more accurate transient and dynamic performance simulations. The parameters of the CNTFET model and their values, with brief descriptions, are shown in Table 2.

Table 2 CNTFET Model Parameters.

Parameter	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT channel	100 nm
L_{dd}	The length of doped CNT drain-side extension region	32 nm
L_{ss}	The length of doped CNT source-side extension region	32 nm
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
Efi	The Fermi level of the doped S/D tube	6 eV
C_{sub}	The coupling capacitance between the channel region and the substrate	20 pF/m

The proposed designs are simulated at room temperature, at 100 MHz and 250 MHz operational frequencies and at 0.9 V supply voltage, which is the standard supply voltage for 32 nm CNTFET technology. Moreover 2fF and 3fF load capacitors are used at the output nodes of the circuits for the simulations. The waveform of the sample input and output signals of the proposed structures are shown in Fig. 6, which authenticates the correct operation of the proposed ternary circuits. The simulation results, including the worst-case delay, the average power consumption and the average energy consumption, are listed in Table 3. According to the simulation results the second proposed

design operates faster that the first one due to its shorter critical path as well as its higher driving capability. The higher driving capability at the Sum node of the second proposed design is because of the shorter path of the output buffer from V_{DD} and GND to the output node. However, it reduces the impedance of the path from V_{DD} to GND and consequently increases the static power consumption and as a result the power consumption of the first proposed design is lower than the second one.

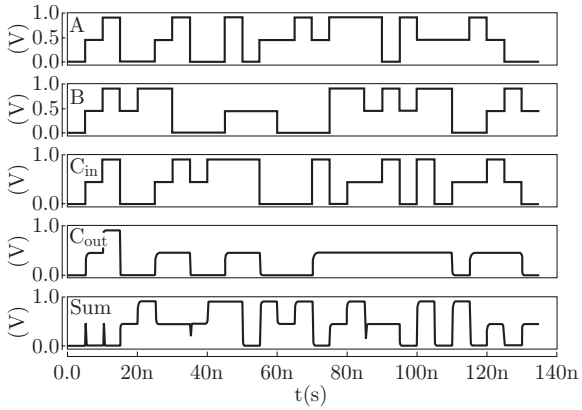

Fig. 6 Waveform of the sample input and output ternary signals.

Table 3 Simulation Results.

Simulation Conditions	Freq=100MHz, Loads=2fF	Freq=250MHz, Loads=3fF
The First Proposed Ternary Full Adder		
Delay ($\times 10^{-10}$ sec)	2.838	3.271
Power ($\times 10^{-6}$ W)	6.361	6.719
Energy ($\times 10^{-15}$ J)	1.806	2.197
The Second Proposed Ternary Full Adder		
Delay ($\times 10^{-10}$ sec)	2.614	2.781
Power ($\times 10^{-6}$ W)	19.71	19.99
Energy ($\times 10^{-15}$ J)	5.152	5.559

As the driving capability is a very considerable parameter, specifically for the fundamental logic and arithmetic circuits, the performance of the circuits are evaluated in the presence of different output load capacitors, ranging from 1fF up to 10fF. The worst-case delay, the average power consumption and the average energy consumption of the proposed circuits are plotted in Fig. 7, 8 and 9, respectively. According to the simulation results, the proposed circuits demonstrate very high driving capability and their delay and power consumption increase a little by increasing the output load capacitances.

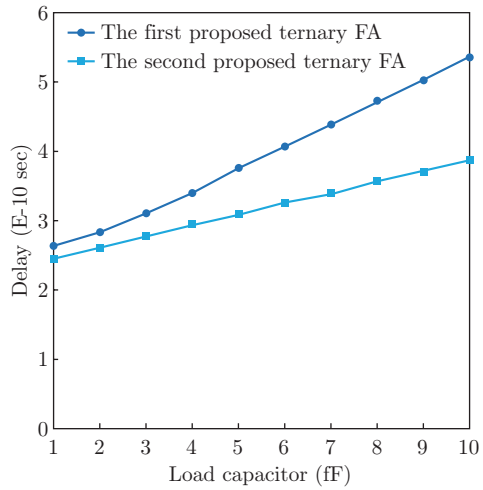

Fig. 7 Delay of the designs versus load capacitors.

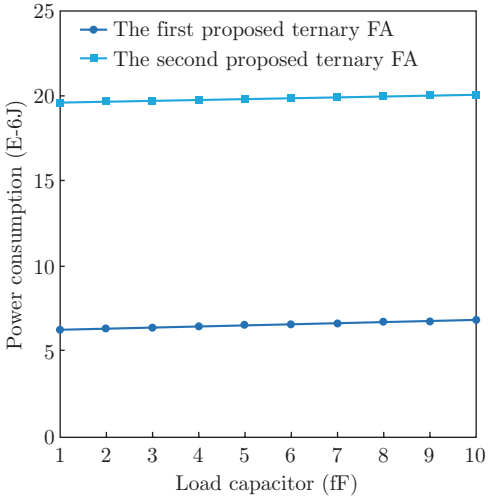

Fig. 8 Power consumption of the designs versus load capacitors.

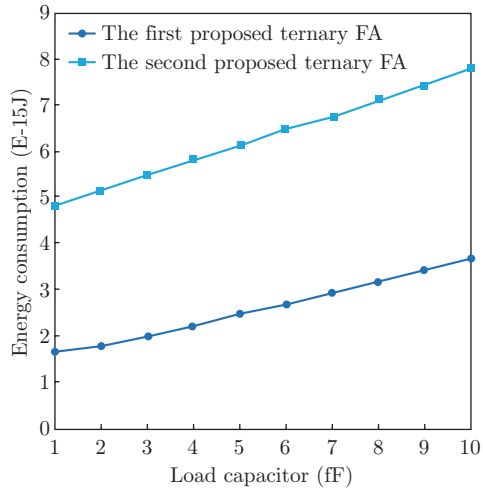

Fig. 9 Energy consumption of the designs versus load capacitors.

Conclusion

Novel efficient ternary Full Adder cells have been proposed for nanotechnology based on the CNTFET devices. The proposed ternary Full Adders have been designed with a new method based on multi-V_{th} nanodevices and have benefited from the unique properties of CNTFET. The presented structures have very high driving capability and decrease the number of the transistors significantly. These new design can be utilized as the building blocks of more complex and larger ternary arithmetic circuits. The proposed ternary Full Adder cells have been simulated using Synopsys HSPICE with 32nm CNTFET technology, which authenticate their correct operation.

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