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High Density 3D Carbon Tube Nanoarray Electrode Boosting the Capacitance of Filter Capacitor

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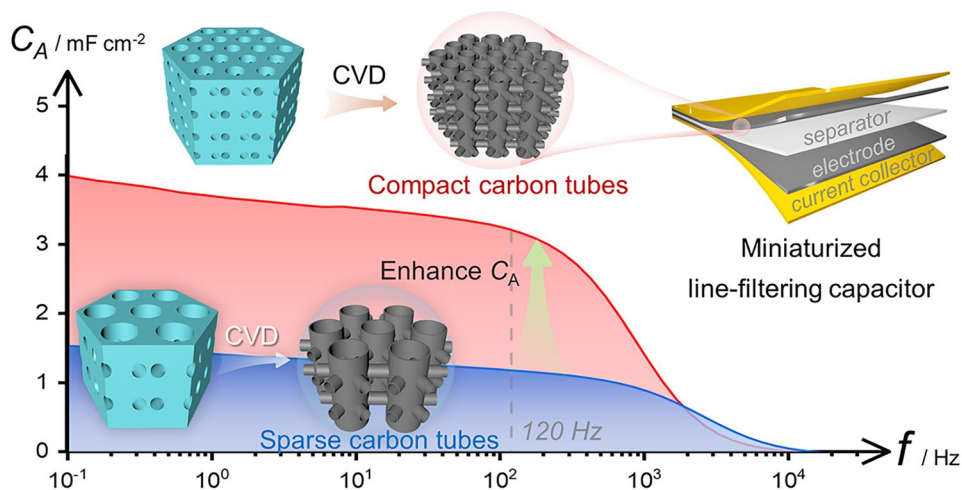
HIGHLIGHTS

- A novel method is developed for precise control over the structure of 3D anodic aluminum oxide templates, enabling fine-tuning of both the vertical pore diameter and interspace within the templates.
- 3D carbon tube nanoarrays featuring significantly thinner and denser tubes are constructed as high-quality electrodes for miniaturized filter capacitors.
- The 3D compactly arranged carbon tube-based capacitor achieves a remarkable specific areal capacitance of 3.23 mF cm^{-2} with a phase angle of -80.2° at 120 Hz.

ABSTRACT Electric double-layer capacitors (EDLCs) with fast frequency response are regarded as small-scale alternatives to the commercial bulky aluminum electrolytic capacitors. Creating carbon-based nanoarray electrodes with precise alignment and smooth ion channels is crucial for enhancing EDLCs' performance. However, controlling the density of macropore-dominated nanoarray electrodes poses challenges in boosting the capacitance of line-filtering EDLCs. Herein, a simple technique to finely adjust the vertical-pore diameter and inter-spacing in three-dimensional nanoporous anodic aluminum oxide

(3D-AAO) template is achieved, and 3D compactly arranged carbon tube (3D-CACT) nanoarrays are created as electrodes for symmetrical EDLCs using nanoporous 3D-AAO template-assisted chemical vapor deposition of carbon. The 3D-CACT electrodes demonstrate a high surface area of $253.0 \text{ m}^2 \text{ g}^{-1}$, a D/G band intensity ratio of 0.94, and a C/O atomic ratio of 8. As a result, the high-density 3D-CT nanoarray-based sandwich-type EDLCs demonstrate a record high specific areal capacitance of 3.23 mF cm^{-2} at 120 Hz and exceptional fast frequency response due to the vertically aligned and highly ordered nanoarray of closely packed CT units. The 3D-CT nanoarray electrode-based EDLCs could serve as line filters in integrated circuits, aiding power system miniaturization.

KEYWORDS Compactly arranged; Three-dimensional carbon tube nanoarray; Dimensional carbon tube nanoarray; Fast frequency response; Electric double-layer capacitors; Layer capacitors; AC line-filtering; Filtering



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1 Introduction

The boom in portable and wearable electronic devices calls for highly integrated circuits and miniaturized components [1–6]. Alternating current (AC)/direct current (DC) conversion is fundamental for powering electronic products [7–9]. Filter capacitors are utilized to smooth the pulse DC voltage after rectification [10–12]. Conventional aluminum electrolytic capacitors (AECs), with bulky size and rigid attributes, dominate the market in the line-filtering field and face the challenges of integrating into miniaturized devices [13–16]. Fast frequency-responsive electric double-layer capacitors (EDLCs) are promising candidates for line-filtering AECs and have attracted extensive attention [17–20]. However, achieving tiny EDLCs with both high energy density and high-frequency response properties remains challenging. The search for high-quality electrode materials with large specific surface areas and efficient electron transport and ion migration paths is critical to developing miniaturized line-filtering EDLCs.

Various novel carbon-based electrode materials for line-filtering EDLCs have been explored [21–28]. Of particular interest are the three-dimensional (3D) upright nanoarrays because of the orientation of the electrode microstructures, which provide smooth ion migration channels [29–33]. However, the fast frequency response of these macropore-dominated electrodes is maintained by sacrificing the energy density, resulting in a low specific areal capacitance (C_A) at 120 Hz, hindering the development of miniaturized line-filtering capacitors [34–36]. Moreover, it is challenging to control the arrangement density of upright nanoarrays using existing methods [22, 37–39]. Therefore, developing a proper way to manage the arrangement of high-orientation nanoarrays to enhance C_A is of great significance.

The nanoporous anodic aluminum oxide (AAO) template-assisted method is suitable for preparing ordered, highly oriented, and uniform nanoarrays with controllable morphology and high repeatability [40–42]. We have constructed 3D carbon tube (3D-CT) grid electrodes fabricated with the help of a unique nanoporous 3D-AAO template-assisted method for high-performance line-filtering EDLCs [8]. The 3D-CTs grid, i.e., a large area of highly-ordered and vertically aligned CTs with the nearest neighboring vertical CTs being interconnected by lateral CTs growing from vertical CTs, holds great potential for fast frequency response and

ultrahigh-power energy storage devices [43–46]. Unfortunately, the sizeable vertical pore diameter (D_p , ~250 nm) and interpore distance (D_{int} , ~450 nm) of the phosphoric acid-anodized 3D-AAO template limit the specific surface area of the resultant 3D-CT grids and, consequently, C_A of the fabricated line-filtering EDLCs. We recently explored 3D multi-layer CT electrodes with a “Russian matryoshka doll” design to increase the specific surface area and C_A for these applications [46]. While these EDLCs achieved significantly enhanced C_A by incorporating smaller coaxial CTs within the larger ones, the fabrication process was very complicated and required stringent control. A more practical approach would be desirable to enhance the vertical-pore density of the 3D-AAO templates directly. This would enable to create 3D-CT arrays with a high packing density of smaller-diameter vertical CTs in a simple 3D-AAO template assisted chemical vapor deposition (CVD) of carbon, leading to a substantial increase in C_A . Up to now, porous 3D-AAO templates have been only achieved by anodizing Al foil with trace impurity in phosphoric acid electrolyte under about 195 V voltage, and with very few specific D_p and D_{int} have been documented [47, 48]. Therefore, it remains challenging to achieve near-continuous control of the vertical pore with small diameter in the nanoporous 3D-AAO templates, and a more in-depth exploration to regulate vertical pore with small diameter in 3D-AAO templates is necessary to increase the density of the resultant vertically aligned 3D-CT arrays and thus enhance the C_A of the 3D-CT nanoarray electrode based line-filtering EDLCs.

Herein, we developed a simple and efficient method to systematically reduce the vertical-pore diameter of the 3D-AAO template by adjusting the anodization conditions, including voltage, electrolyte composition, and temperature. Consequently, compared with those of the phosphoric acid anodized 3D-AAO template under 195 V, the vertical pore diameter D_p and interpore distance D_{int} of the new 3D-AAO template can be continuously adjustable to smaller ones of 70–250 and 110–450 nm, respectively. We used these new 3D-AAOs with smaller D_p and D_{int} as templates to prepare 3D compactly arranged CT (denoted as 3D-CACT) nanoarrays via the CVD method. The ordered 3D-CACT nanoarrays with tightly packed CT units provide rich and accessible specific surface area and rapid ion transport paths, making it a high-quality electrode for line-filtering EDLCs, resulting in a high C_A of 3.23 mF cm⁻² and a phase angle of -80.2° at 120 Hz, and exhibiting great potential for compact

line-filtering applications. The 3D-CACT-based EDLCs can function as filter capacitors in integrated circuits, contributing to the miniaturization of power transmission systems.

2 Experimental Section

2.1 Materials

Commercial Al foils with a purity of 99% and a thickness of 0.1 mm were purchased from Shanghai Dingxin Materials Co., Ltd. (China). Other chemicals and reagents, including concentrated phosphoric acid (H_3PO_4), oxalic acid ($\text{H}_2\text{C}_2\text{O}_4$), sulphuric acid (H_2SO_4), tin tetrachloride (SnCl_4), hydrofluoric acid (HF), were supplied from Sinopharm Chemical Reagent Co., Ltd. (China).

2.2 Preparations of 3D-AAOs and 3D-CTs

2.2.1 Preparations of the 3D-AAO Templates

Using 0.3 M phosphoric acid (H_3PO_4) solution as the electrolyte, Al foil with Cu impurities (99% purity, 100 μm thick) as the positive electrode, graphite as the negative electrode, the anodic oxidation was carried out at 0 °C and a DC constant voltage of 195 V. The anodizing duration could control the thicknesses of 3D-AAO templates. The remaining aluminum (that had not been anodized) was removed in a saturated tin tetrachloride (SnCl_4) solution, then, the sample was immersed in a 5 wt% H_3PO_4 solution at 40 °C for 15 min to obtain the 3D-AAO templates with large vertical pore diameter D_p and interpore distance D_{int} . To achieve reduced vertical pore diameter D_p and interpore distance D_{int} in 3D-AAO templates, a combination of lower anodization voltage and a suitable electrolyte is necessary. The smallest D_p and D_{int} were obtained using a 0.3 M oxalic acid ($\text{H}_2\text{C}_2\text{O}_4$) solution at 10 °C and an anodization voltage of 50 V. For a broader range of D_p and D_{int} values, a mixed electrolyte (0.1 M $\text{H}_2\text{C}_2\text{O}_4$ +0.05 M H_3PO_4) at 10 °C was employed with anodization voltages of 55, 65, 85, 105, 125, 140, and 155 V.

2.2.2 Preparations of the 3D-CT Nanoarrays

The as-prepared 3D-AAO templates were first placed into a horizontal furnace and heated to 1000 °C at 10 °C min^{-1} under an Ar atmosphere. Then, the carbon tubes were grown on the pore walls of the template by pyrolyzing acetylene at 1000 °C, with a flow gas C_2H_2 at 60 standard cubic centimeters per minute (sccm) under the pressure of -0.1 MPa. The resultant samples were then cleaned by Ar plasma with a Plasma Cleaner (Harrick Plasma, PDC-32G) for 30 min to remove the surface amorphous carbon layer and then immersed in 40 wt% hydrofluoric acid solution for 48 h to selectively remove the AAO templates. Finally, after several rinses in deionized water, the 3D-CT nanoarrays were achieved.

2.3 Assembly of EDLCs

For the aqueous system, the symmetrical EDLC was assembled using two identical 3D-CT nanoarrays (the area of each piece is about 0.09 cm^2) as electrodes, platinum sheets as current collectors, 1 M H_2SO_4 as the electrolyte, and the NKK-MPF30AC-100 film as the separator. For the organic system, the electrolyte and the separator were replaced by 1 M tetraethylammonium tetrafluoroborate (TEA-BF_4 , Sigma-Aldrich) dissolving in dry acetonitrile (Sigma-Aldrich) and NKK-TF4030, respectively. Subsequently, the assembled prototype devices were packaged with polyethylene terephthalate (PET) films.

3 Results and Discussion

3.1 Design Strategy and Structural Characterizations

The concept of regulating the vertical pore diameter D_p and interpore distance D_{int} of 3D-AAO templates to increase the CT density of the resultant CVD 3D-CTs nanoarray is illustrated in Fig. 1. The conventional method for preparing 3D-AAO template involves anodizing aluminum foil containing trace impurities with a 0.3 M phosphoric acid solution as an electrolyte at 0 °C under a high voltage of 195 V. The resulting porous 3D-AAO with large vertical pore diameter D_p (~ 250 nm) and large vertical-pore interspacing D_{int} (~ 450 nm) is used as a template, followed by CVD to obtain a 3D Sparsely Arranged CT (denoted as 3D-SACT)

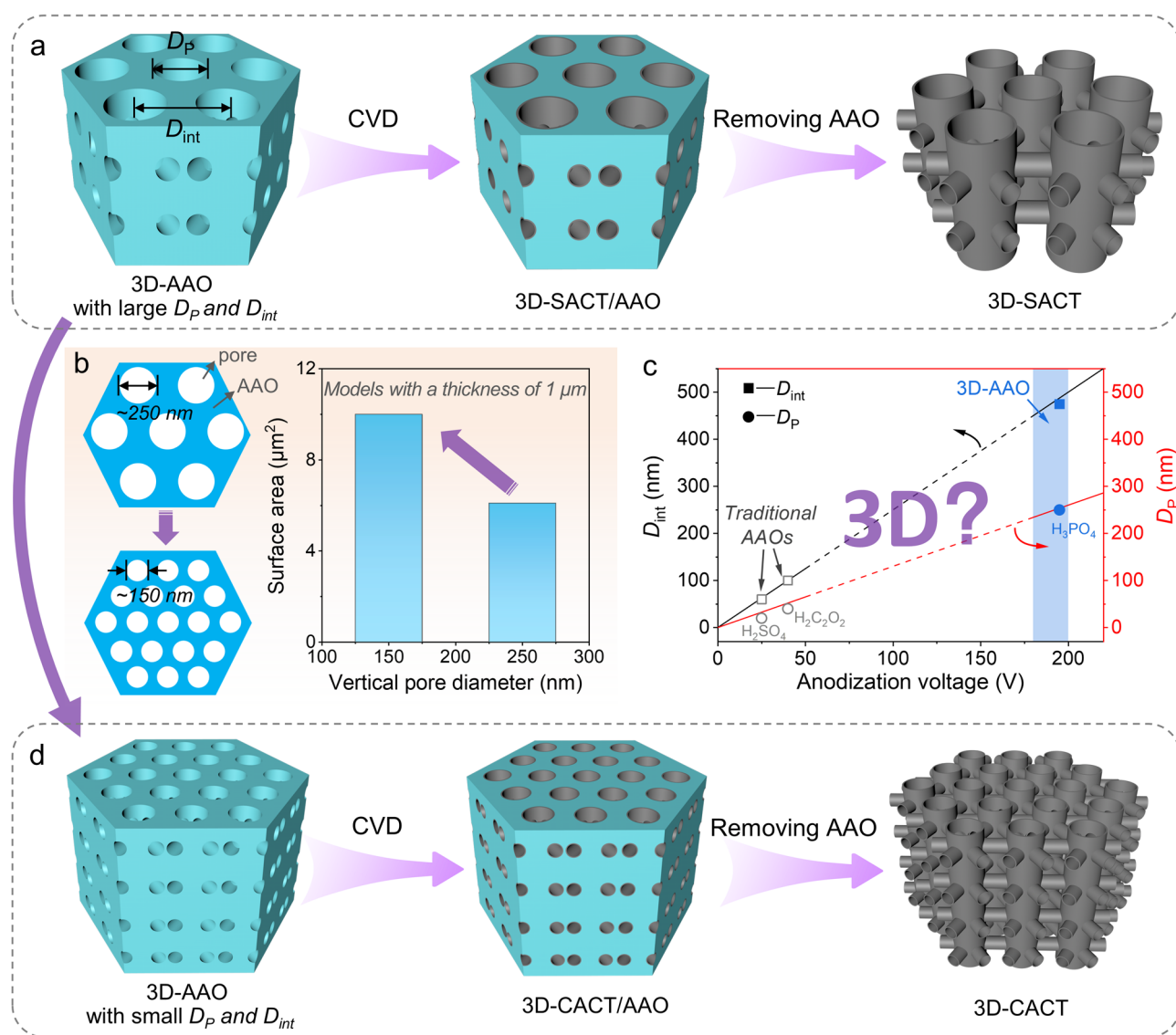


Fig. 1 Schematic illustration of concepts and synthesis processes for 3D-SACT and 3D-CACT. **a** Preparation of 3D-SACT using a 3D-AAO template with large D_p and D_{int} . **b** Plots of pore surface area for two ideal AAO models vs. vertical pore diameter. **c** Plots of vertical D_p and D_{int} of the AAO vs. anodization voltage. **d** Preparation of 3D-CACT using a 3D-AAO template with small D_p and D_{int}

nanoarray after removing the AAO (Fig. 1a). However, this macropore-dominated 3D-CT nanoarray exhibits inefficient space utilization, resulting in a lower specific surface area. By simultaneously reducing both the vertical pore diameter D_p and interpore distance D_{int} , the pore surface area of the AAO template can be effectively enhanced (Fig. 1b). This, in turn, leads to a substantial increase in the specific surface area of the resultant CT nanoarray. Traditionally, achieving this requires lowering the anodization voltage based on the well-established linear relationship between pore structure

and voltage observed in traditional AAO templates. However, existing methods for preparing traditional straight-pore AAO templates at low voltages (< 185 V, Fig. 1c) are not directly applicable to fabricating 3D-AAO templates with lateral pores. This limitation presents a challenge in obtaining 3D-AAO templates with both small D_p and D_{int} . This ability is critical for producing the 3D-CACT with high CT density and specific surface area (Fig. 1d).

This goal is achieved by rational controlling anodization parameters such as voltage, electrolyte composition, and

temperature. Traditionally, low voltage anodization leads to small D_p and D_{int} , and the acidic electrolyte should be replaced to match the voltage window, for example, usually 25 V anodization for 0.3 M sulphuric acid, 40 V anodization for 0.3 M oxalic acid, and 195 V anodization for 0.3 M phosphoric acid. Herein, we used Al foil with trace Cu impurity as the starting material to prepare the 3D-AAO template and utilized 0.3 M sulphuric acid as the electrolyte and anodized at 0 °C under 25 and 30 V, respectively. The experiment results show that there are almost no lateral pores under the voltages lower than 30 V (Fig. S1), which could be ascribed to the fact that a relatively high voltage is required to drive Cu impurities accumulation in the AAO pore wall during the anodization [47]. Then, we used 0.3 M oxalic acid as the electrolyte and anodized at 10 °C under 40, 45, and 50 V, respectively. It was observed that when the voltage was lower than 50 V, fewer lateral pores were formed (Fig. S2), reaffirming that a high voltage is needed to anodize Al foil with trace Cu impurity to form lateral pores in the preparation of the 3D-AAO template. Therefore, when oxalic acid is used, the 3D-AAO templates should be prepared under a high voltage of over 50 V. Subsequently, a mixed electrolyte of oxalic acid and phosphoric acid is used to bridge the voltage gap between 50 and 195 V. As a result, 3D-AAO templates with smaller vertical pore diameter D_p and interpore distance D_{int} were successfully prepared at voltages of 50–155 V. Using these new 3D-AAO templates, 3D-CTs with different vertical tube diameters and inter-tube spacings were fabricated via CVD processes.

3D-AAO templates anodized at different voltages (denoted as O-50 V-AAO, M-55 V-AAO, M-65 V-AAO, M-85 V-AAO, M-105 V-AAO, M-125 V-AAO, M-140 V-AAO, M-155 V-AAO, and P-195 V-AAO, where the capital letters O, P, and M represent oxalic acid, phosphoric acid electrolyte, and their mixture, respectively, and the Arabic numbers represent the anodizing voltages) exhibit similar pore structures, characterized by interconnected vertical and lateral pores (Figs. S3 and S4). Interestingly, the corresponding resultant 3D-CT nanoarrays become progressively denser with the anodization voltage decrease (Fig. 2a–e). Analysis of digitally processed scanning electron microscope (SEM) images yielded the distributions of vertical pore diameter D_p and interpore distance D_{int} , presented in Figs. 2f, g and S4i, j. For P-195 V-AAO, vertical D_p and D_{int} were approximately 250 nm and 450 nm, respectively. Anodization in mixed acid at 155, 105, and 65 V led to

progressively smaller vertical D_p (around 200, 150, and 110 nm) and D_{int} values (about 350, 250, and 130 nm). O-50 V-AAO displayed the smallest vertical D_p (70 nm) and D_{int} (110 nm). Remarkably, the vertical pore diameter D_p and interpore distance D_{int} exhibit an almost linear decrease with the anodizing voltage decrease across the range from 195 to 50 V (Fig. 2h). The 3D-CT nanoarrays faithfully replicate the morphology of the 3D-AAO templates well (denoted as 3D-CT-O-50 V, 3D-CT-M-55, -65, -85, -105, -125, -140, and -155 V, and 3D-CT-P-195 V, respectively, Figs. 2i and S5, S6). Furthermore, the 3D-CT nanoarrays were characterized by Raman and X-ray photoelectron spectroscopy (XPS) spectra, displaying low D/G band and O/C intensity ratios (Fig. S7) [49]. The Braunauer–Emmett–Teller (BET) surface areas of 3D-CT-P-195 V and 3D-CT-M-65 V calculated from the nitrogen adsorption–desorption isotherms were increased from 94.1 to 253.0 m² g⁻¹, demonstrating that reducing the vertical D_p and D_{int} plays a crucial role in improving the specific surface area (Fig. S8) [50]. Compared to the previously reported 3D-CT-based electrodes, the preparation process of high-quality 3D-CACT electrodes is more efficient and straightforward.

3.2 Electrochemical Performance

After assembling two identical 3D-CT nanoarrays as electrodes and using a 1 M sulfuric acid solution as the electrolyte, along with two pieces of Pt foils as the current collectors, the symmetrical EDLCs were constructed (Fig. 3a). The 3D-CTs of 3D-CT-O-50 V, 3D-CT-M-65 V, 3D-CT-M-105 V, 3D-CT-M-155 V, and 3D-CT-P-195 V with the same thickness of approximately 12 μm were used as electrodes (Fig. S9). Finite element simulation results show that the structure of the 3D-CT can maintain good stability under the pressure of the fixture during the electrochemical performance test (Fig. S10). Electrochemical impedance spectroscopy (EIS) measurements were conducted to assess the frequency response of the 3D-CTs nanoarray-based EDLCs.

The phase angle, as a function of frequency, is plotted in Fig. 3b. The closer the phase angle reaches -90°, the more capacitive behavior the device exhibits [12, 51]. At low frequencies, all the EDLCs exhibit favorable capacitive behavior. The phase angles at 120 Hz of the 3D-CT-O-50 V-, 3D-CT-M-65 V-, 3D-CT-M-105 V-, 3D-CT-M-155 V-, and 3D-CT-P-195 V-based EDLCs achieve -79.2°, -80.2°, -8

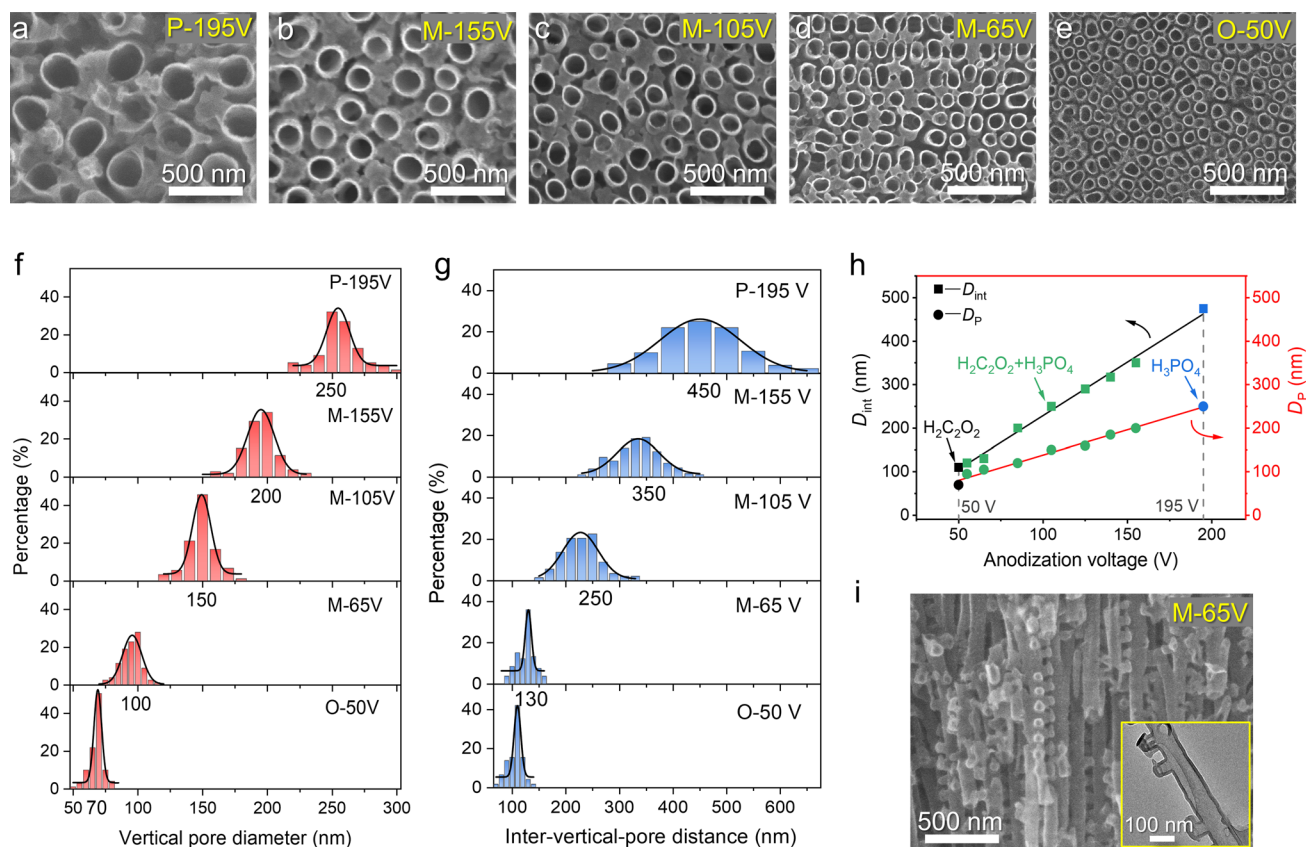


Fig. 2 Morphological and structural characteristics of the 3D-AAOs and 3D-CTs with different vertical pore/tube diameters and spacing. Top-view SEM images of **a** 3D-CT-P-195 V, **b** 3D-CT-M-155 V, **c** 3D-CT-M-105 V, **d** 3D-CT-M-65 V, and **e** 3D-CT-O-50 V. The vertical **f** D_p and **g** D_{int} distribution diagram. **h** Plots of vertical D_p and D_{int} of the 3D-AAO vs. anodization voltage. **i** Typical cross-sectional SEM image of 3D-CT-M-65 V. The inset shows its transmission electron microscope (TEM) image

1.3° , -81.9° , and -83.3° , respectively. Most of the values of phase angles at 120 Hz are comparable to that of a commercial AEC (330 $\mu\text{F}/6.3$ V, Panasonic, Japan, Figs. 3b and S11), indicating the sufficiently fast frequency response of the 3D-CT-based EDLCs. Moreover, as the diameter of the vertical CTs decreases, the pore size in the 3D-CT nanoarray electrode also decreases, leading to a narrowing of the ion transport paths and an increase in the phase angle. The frequency at the phase angle of -45° ($f_{.45}$), recognized as the cutoff value to distinguish the capacitive and resistive nature of an EDLC [15], reaches 754, 957, 1211, 1539, and 2431 Hz for the above EDLCs (Fig. 3b), respectively. The straight lines are almost parallel to the imaginary axis at low frequencies in the Nyquist plots (Fig. 3c), revealing ideally capacitive characteristics [52]. The absence of the 45° oblique line in the low-frequency region and semicircle in the high-frequency region suggest efficient electron

conduction [53, 54]. The equivalent series resistance (ESR) values were all estimated to be less than $0.07 \Omega \text{ cm}^2$ (the size of the electrodes is $0.3 \times 0.3 \text{ cm}^2$), implying excellent electric conductivity and low internal resistance of the electrodes, as well as good interfacial contact between the electrodes and current collectors [14, 17].

A series resistor–capacitor (RC) circuit model was used to simulate the device elements. The real (C') and imaginary (C'') capacitances of the devices, extracted from the EIS spectra, are presented in Figs. 3d and S12. The areal capacitance C' represents the accessible energy storage capacitance at the corresponding frequency and is used to characterize the C_A . At 120 Hz, the C_A of the 3D-CT-O-50 V-, 3D-CT-M-65 V-, 3D-CT-M-105 V-, 3D-CT-M-155 V-, and 3D-CT-P-195 V-based EDLCs reaches 4.11, 3.23, 2.01, 1.73, and 1.18 mF cm^{-2} , respectively. The C_A can also be obtained from the cyclic voltammetry (CV) and galvanostatic

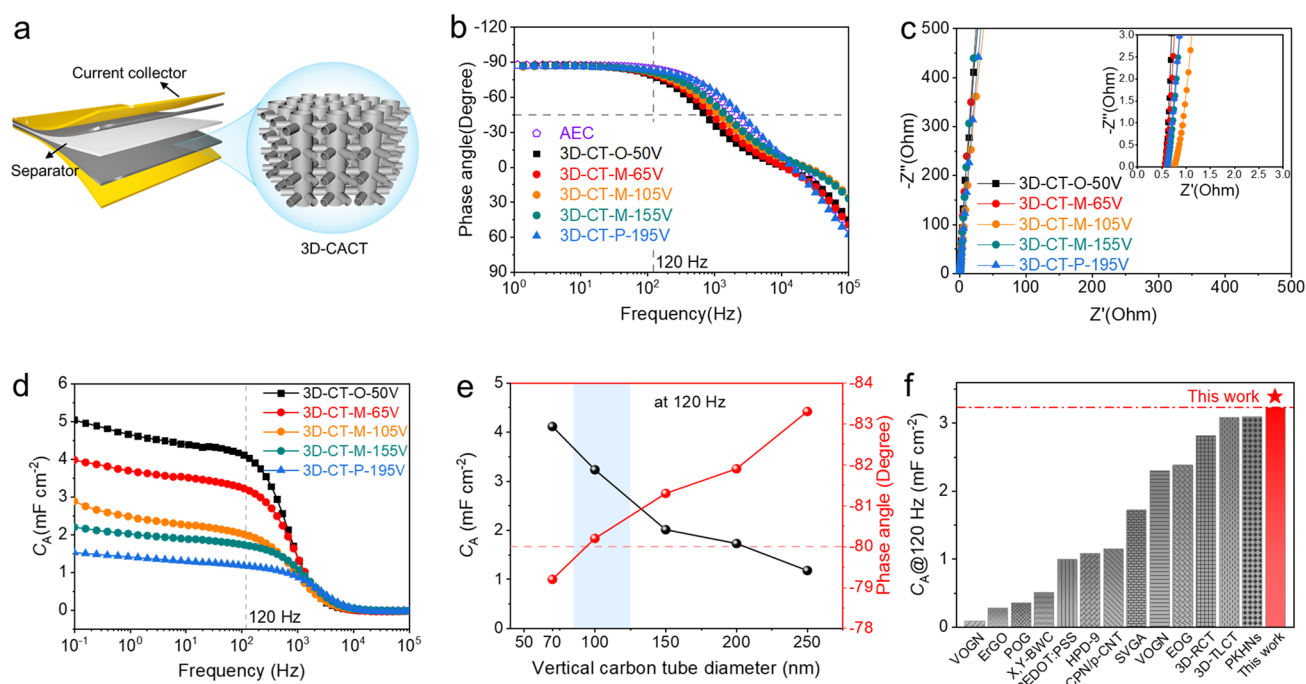


Fig. 3 Electrochemical performances of the 3D-CT-O-50 V-, 3D-CT-M-65 V-, 3D-CT-M-105 V-, 3D-CT-M-155 V-, and 3D-CT-P-195 V-based EDLCs. **a** Schematic illustration of the 3D-CT nanoarray-based EDLC. **b** Bode plots of the above devices and AEC (330 $\mu\text{F}/6.3$ V, Panasonic, Japan). **c** Nyquist plots, the inset shows the expanded view at high frequencies. **d** Frequency-dependent areal capacitance (C_A) of the 3D-CT-O-50 V-, 3D-CT-M-65 V-, 3D-CT-M-105 V-, 3D-CT-M-155 V-, and 3D-CT-P-195 V-based EDLCs. **e** Plots of C_A and phase angles at 120 Hz vs. vertical CT diameter. **f** Comparison of the C_A at 120 Hz of 3D-CT-M-65 V-based EDLC and other reported sandwich-type electrochemical capacitors used in the AC filter circuits with the phase angle near or less than -80°

charge–discharge (GCD) tests, which show similar value magnitudes (Fig. S13). The 3D-CT-M-65 V-based EDLC exhibits a C_A value of 3.23 mF cm^{-2} at 120 Hz, almost tripling that of the 3D-CT-P-195 V-based EDLC. This dramatic increase highlights the significant impact of high-density 3D-CT nanoarray electrodes in enhancing the capacitance of line-filtering EDLCs. Notably, this C_A value is the highest among all the sandwich-type filtering EDLCs reported to date with a phase angle lower than -80° at 120 Hz (Fig. 3e, f, Table S1). The specific volumetric capacitance C_V at 120 Hz can approach 1.71 F cm^{-3} for the 3D-CT-O-50 V electrode (Fig. S14a).

From the frequency (f_0) at which the C'' reaches the maximum value, the relaxation time constant τ_0 ($\tau_0 = 1/f_0$) can be derived, which represents the minimum time required for discharging with an energy efficiency of over 50% [34, 55]. The τ_0 at 120 Hz is calculated to be 1.33, 1.04, 0.83, 0.65, and 0.41 ms, respectively. The relatively short time means a fast discharge characteristic. The RC time constant (τ_{RC}) is a critical parameter reflecting the charging/discharging speed

[35, 56]. The τ_{RC} values are measured to be 0.28, 0.25, 0.27, 0.2, and 0.17 ms at 120 Hz, comparable to AEC (0.14 ms), demonstrating the highly efficient reduction of charging/discharging time for high-rate performance and rapid frequency response. The frequency-dependent C'/C values are close to 1 at 120 Hz (Fig. S14b), suggesting less excessive energy loss and high actual energy storage efficiency [57]. The degree of energy loss as heat dissipation can be reflected by the evolution of the dissipation factor (DF) with the frequency [26]. The relatively low DF at 120 Hz of the EDLCs mentioned above manifests the characteristic of little energy loss (Fig. S14c).

The ideal capacitive behavior and the ultrafast ion adsorption and transport performance of the 3D-CT-M-65 V-based EDLCs were further investigated through CV and GCD tests. The near quasi-rectangular shapes of the CV curves were maintained even at the scan rate of 1000 V s^{-1} , as shown in Fig. S15a, b, and a linear relationship of discharge current density with the scan rates up to 1000 V s^{-1} is presented (Fig. S15c), suggesting ultrafast charging/discharging and

excellent rate capabilities within the electrodes. These characteristics were also verified by GCD tests (Fig. S15d–f), in which all the curves are close to triangular curves, and the derived specific capacitances show stable retention under high current densities. Furthermore, the 3D-CT-M-65 V-based EDLC exhibits excellent electrochemical cycle stability, as evidenced by the nearly 98% capacitance retention and 100% coulombic efficiency after 12,000 cycles at the current density of 10 mA cm^{-2} (Fig. S16). The phase angle at 120 Hz remains almost unchanged during the charge/discharge process.

To fabricate capacitor banks with high operating voltage, integrating EDLC units is critical for multifunctional practical applications [29]. Six and ten 3D-CT-M-65 V-based EDLC units, each with an electrode area of approximately 1 cm^2 and a thickness of $8.5 \mu\text{m}$, were connected in series to benchmark AECs operating at 6.3- and 10-V (Figs. S17 and S18). The capacitor banks exhibited stable and excellent electrochemical performance, as verified by EIS, CV, and GCD tests. Compared with the single device (-81.2°), the phase angles of six or ten devices in series at 120 Hz increase slightly, reaching about -81.0° and -80.6° , respectively (Fig. 4a), indicating that the integrated capacitor banks still have excellent frequency response comparable to the

rated AECs. The nearly vertical line features in the low-frequency region in the Nyquist plots indicate typical capacitive behaviors of the devices in series (Fig. 4b). The ESR of six or ten devices in series is around 6 or 10 times of a single device (Table S2).

Moreover, the six and ten EDLC units in series display almost the same relaxation time τ_0 as that of the single device (Fig. 4c); this is mainly due to the stability of the structure and electrochemical properties of the nanoarray electrodes, the close electrical contact between electrodes and current collectors, and between the units. The C_A of a single device is approximately 6 and 10 times that of six and ten devices in a series. The C'/C values are close to 1, and the DF is steady at a low value at 120 Hz (Fig. 4d), suggesting the almost lossless energy and fast frequency response performance. Besides, the quasi-rectangular shapes of CV curves and symmetrical triangular shapes of GCD curves are maintained well (Fig. 4e, f), implying the high reproducibility and high power and rate capability of fabricated EDLC units under different external voltages. All of these demonstrate the stability and homogeneity of the 3D-CACT-based EDLCs for constant performance after series connection.

The operating voltage of the 3D-CT-M-65 V-based EDLC could be further broadened by increasing the number of

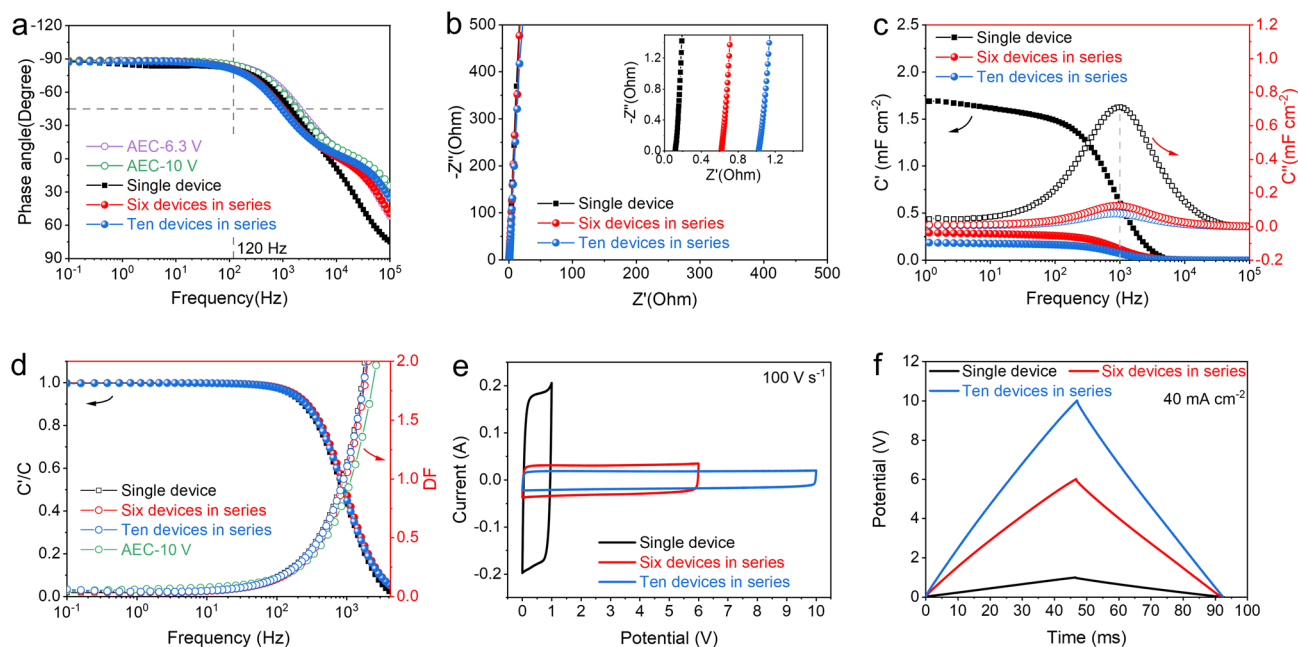


Fig. 4 Electrochemical performances of single EDLC, six and ten EDLCs in series. **a** Bode plots. **b** Nyquist plots. **c** Real and imaginary parts of capacitance versus frequency. **d** Variations of C'/C and DF versus frequency. **e** CV curves and **f** GCD curves

units in series or using an organic electrolyte. The specific volumetric capacitance at rated voltage ($C_{V\ vol}$) of the 3D-CT-M-65 V-based EDLC was compared with commercial AECs [58]. The calculated $C_{V\ vol}$ in the aqueous electrolyte is $0.24/V^2$, where V is the voltage rating (based on the volume of the device, Supporting Information). The device with organic electrolyte also shows high capacitive and filtering performance (Figs. S19 and S20), with the $C_{V\ vol}$ increasing to $0.96/V^2$. The 3D-CT-M-65 V-based EDLCs could have a higher volumetric capacitance than commercial AECs up to ~ 25 V in the aqueous electrolyte and ~ 160 V in the organic electrolyte, respectively (Fig. S21), indicating that they could replace AECs for low voltage (< 160 V) AC line-filtering.

3.3 AC Line-Filtering Performance

To demonstrate realistic AC line filtering, we connected ten devices in series to filter the sinusoidal AC signal into a smooth DC signal. The filter circuit is equipped with 3D-CT-M-65 V-based EDLCs, a rectifier, and a loading resistance

(R_L) of 10 k Ω as illustrated in Fig. 5a. A 60 Hz AC input signal (with voltage peak to peak of 20 V) was converted to a 120 Hz DC signal via a rectifier (Fig. 5b). Subsequently, the pulsating DC signal was smoothed to a DC output with trivial voltage fluctuation after passing through the capacitors, comparable to a commercial AEC (10 V/100 μ F, Nippon, Japan). The capacitors in series show comparable output voltages and small variance coefficients compared with AECs under different R_L values (Fig. S22). Furthermore, this circuit effectively filters square, triangular, arbitrary, and noise waveform ripples, demonstrating its potential for diverse filtering requirements (Fig. S23). These results indicate that the 3D-CACT-based electrode, with sufficient specific surface area, smooth ion channels, and high conductivity, can effectively facilitate ion adsorption/desorption. It shows significant potential to replace bulky AECs in AC line-filtering. In addition to AC power signals, the discontinuously pulsating AC output from a rotating disk triboelectric nanogenerator (RD-TENG) can be efficiently smoothed using the rectifying and filtering circuit with a capacitor bank. The RD-TENG consists of a stator printed

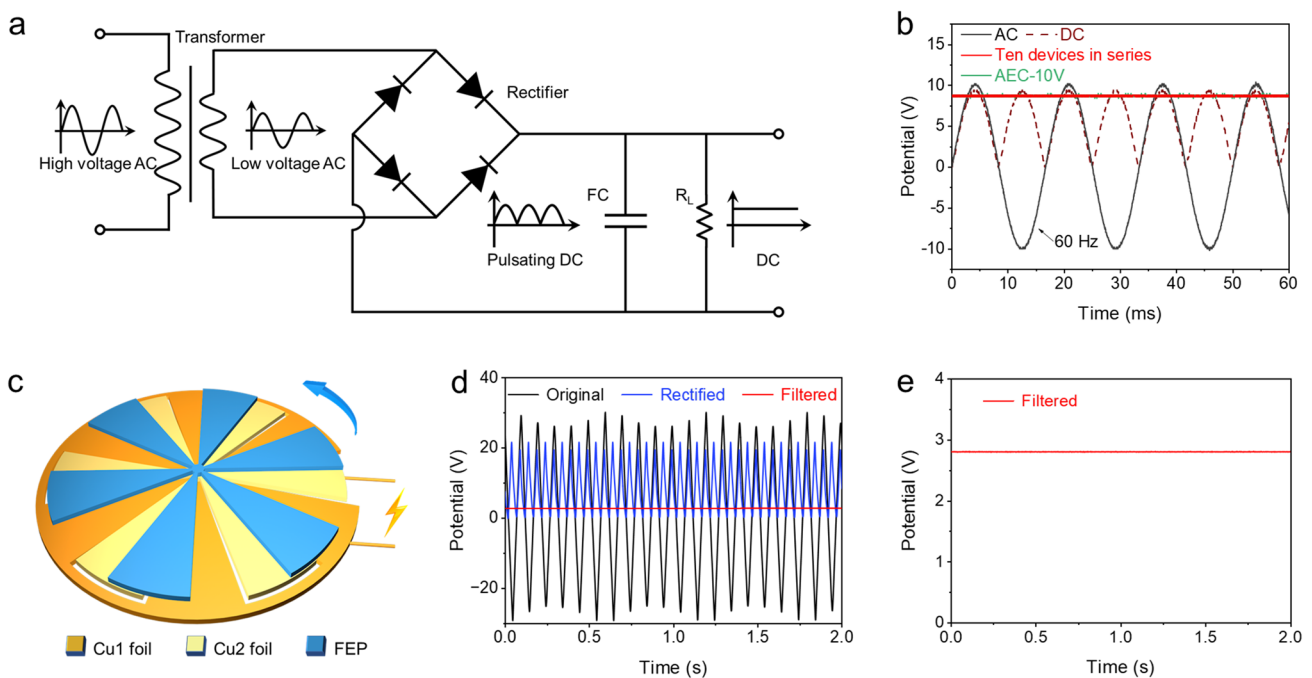


Fig. 5 AC line-filtering performance demonstration. **a** Schematic demonstration of the rectifying and filtering circuit. The rectifier is built with four silicon Schottky diodes (1N5824, Master Instrument Corporation). **b** AC line-filtering results of the ten EDLCs in series and a commercial AEC (10 V/100 μ F, Nippon, Japan) with R_L of 10 k Ω . **c** Schematic illustration of the basic structure of the RD-TENG composed of the FEP layer and the stationary Cu layer. **d** Electrical signals powered by TENG at the initial AC, rectified, and filtered DC states. **e** Filtered signal

with a copper pattern and a rotor made of fluorinated ethylene propylene (FEP) film (Fig. 5c) [15]. The filtering capacitor banks were achieved by connecting ten devices in series. The signals from the RD-TENG, the rectifier, and the capacitors are shown in Fig. 5d, respectively. A stable DC output voltage with almost no ripples and attenuation was obtained after rectification and filtering (Fig. 5e), demonstrating the outstanding pulse smoothing ability of the filtering capacitor banks [59]. Furthermore, the capacitors can rapidly absorb the limited charge generated by the RD-TENG, effectively safeguarding them from damage caused by transient high voltages [60]. The excellent filtering performance suggests that replacing AECs with 3D-CACT-based EDLC banks would significantly improve the practicability of miniaturizing distributed energy harvesting equipment, self-power systems, and wearable electronics.

4 Conclusions

In summary, we fabricated a structurally integrated 3D-CT nanoarray with tunable vertical CT density by simultaneously regulating the vertical pore diameter D_p from 70 to 250 nm and interpore distance D_{int} from 110 to 450 nm of the 3D-AAO template. The resultant 3D-CACT nanoarray with smaller diameter and denser CTs exhibits significantly increased specific surface area and maintained rapid ion transport paths, leading to a high C_A of 3.23 mF cm^{-2} for sandwich-stacked EDLCs and a phase angle of -80.2° at 120 Hz, exhibiting excellent line-filtering performance. Moreover, the structure-adjustable template auxiliary method holds great potential for customizing the size of nanomaterials and developing integrated microdevices.

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Declarations

Conflict of interest The authors declare no interest conflict. They have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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